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PERSPECTIVE

Patterning graphene nanostripes in substrate-supported functionalized graphene: A promising route to integrated, robust, and superior transistors

Liang-feng Huang, Zhi Zeng†

Key Laboratory of Materials Physics, Institute of Solid State Physics, Chinese Academy of Sciences, Hefei 230031, China

E-mail: †zzeng@theory.issp.ac.cn

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It is promising to apply quantum-mechanically confined graphene systems in field-effect transistors. High stability, superior performance, and large-scale integration are the main challenges facing the practical application of graphene transistors. Our understandings of the adatom-graphene interaction combined with recent progress in the nanofabrication technology indicate that very stable and high-quality graphene nanostripes could be integrated in substrate-supported functionalized (hydrogenated or fluorinated) graphene using electron-beam lithography. We also propose that parallelizing a couple of graphene nanostripes in a transistor should be preferred for practical application, which is also very useful for transistors based on graphene nanoribbon.

Keywords graphene nanostripe, functionalized graphene, field-effect transistor

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Since the first fabrication and measurement of graphene in 2004 [1], it has become promising in the fields of materials, chemistry, physics, and biology, due to its superior mechanical, electronic and optical properties, low mass density, controllable synthesis, biological compatibility, and so on [2–11]. Graphene transistor is an important application of graphene in these fields, which recently has drawn tremendous interest from both the scientific and industrial communities. The bulk graphene is a semimetal, and a band gap should be created to achieve high on/off (signal/noise) ratio in graphene transistors [12].

• *High stability, atomically sharp edges, substrate decoupling, and large-scale integration are required for the practical application of graphene nanostructures in field-effect transistors.*

Quantum-mechanically confining the carriers in graphene nanoribbon (GNR) is an effective and controllable way for the band-gap engineering [13–18]. GNRs currently have been fabricated through masked plasma etching [13, 14], chemical derivation [15, 16], unzipping carbon nanotubes [17, 18], nanoparticle etching [19], surface-assisted self-assembly [20], templated self-organization [21], and nanoimprint lithography [22]. The band gap of GNR increases inversely with the ribbon width, and a sub-10-nm width is required for a satisfactory on/off ratio in a GNR-based field-effect transistor (GNR-FET) under conventional conditions [14, 16, 18, 22]. Presently, only the masked-plasma etching method has successfully integrated sub-10-nm GNRs on semiconductor substrate [23]. However, the electronic performance of narrow GNRs is still significantly affected by the edge disorder (caused by the high-energy plasma etching), chemical bonding with unexpected adsorbates, and many detrimental effects from the substrate (additional carrier scattering, intrinsic charge doping, parasitic capacity, and unpredictable disorder-induced gap) [15, 24–28]. Probably due to some edge disorder [29], the theoretically predicted spin-polarized transport in zigzag-GNR [30] has not been experimentally observed. Thus, further improvement in the fabrication of GNR is still required to overcome these obstacles for its practical usage. In addition, large-scale integration is also required for the application of GNR in semiconductor industry.

As a counterpart of GNR, the quasi-one-dimensional graphene nanostripe (GNS) sculptured in functionalized (hydrogenated or fluorinated) graphene (FG) has the similar electronic structure as that of GNR, and is regarded as another promising candidate for FET [31–

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35]. To obtain superior electronic performance, the edges of GNS, namely the graphene/FG interfaces, should be sharp enough down to the atomic scale, and the fabricated GNS should be robust (without structural changing for a very long time) under conventional conditions. Furthermore, to be an alternative or even a substitute of present silicon-based FETs, large-scale integration of GNS-FET should be readily realized. Scanning-probe lithography is a powerful and miniature electron-beam lithography, which can fabricate nanostructures on surfaces with dimensions even down to several nanometers [36]. This method could be used to sculpture sub-10-nm GNSs in FG. The sculpturing process is designed as shown in Fig. 1, in which a GNS is sculptured out in a substrate-supported FG sheet by using a biased scanning probe. The C–X bonds (X is H or F) at the graphene/FG interfaces are broken by the electron-beam excitation. The molecules desorbed upward will escape into vacuum with high escaping velocity, while those downward tend to dissociate again and be adsorbed onto the semiconductor substrate [35]. Those adatoms on the substrate prevent the GNS from covalently bonding with the substrate [37–39], which can guarantee the superior electronic performance of the fabricated GNS. Through systematically simulating the kinetics of the adatoms at various graphene/FG interfaces [35], we have shown that it is probable to sculpture GNSs with sharp and highly-stable edges in FG. This is because of the considerable increase of the reactivity of the C atoms to H (or F) adatoms with changing the adsorption site from sp^2-hybridized GNS to sp^3-FG [35, 40, 41]. Furthermore, scanning-probe lithography should be capable of integrating GNSs in FG [36], which is schematically shown in Figs. 2(a) and (b). Neighboring GNSs can be easily decoupled by just couples of adatom lines [42], which indicates that the GNSs could be sculptured very close to but without influencing each other. Thus, high-density integration of GNSs can be realized in FG. In addition, the edges of the experimentally fabricated GNSs in hydrogenated [43] and fluorinated graphene [44] are still not atomically sharp, which is probably due to the fact that the adatom coverage is not high enough in these two experiments [35]. Thus, to obtain sharp-edge GNSs, it is critical to have FG sheets with high enough adatom coverage.

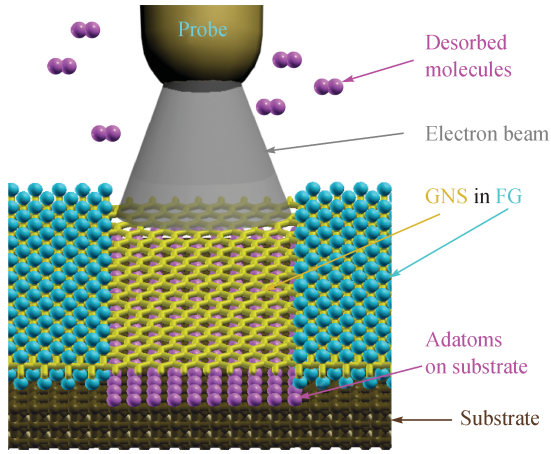

Fig. 1 The schematic drawing of the sculpturing of a GNS in a substrate-supported FG sheet by electron-beam lithography. The electron beam is generated using a biased scanning probe.

• *Parallelizing a couple of GNSs in a FET can make the integrated GNS-FETs perform uniformly and be immune to small structural and environmental perturbations, which also could be generalized to GNR-FET.*

After sculpturing a GNS in a substrate-supported FG sheet, a GNS-FET can be achieved by depositing the source and drain electrodes, dielectrics, and gate electrode, subsequently. However, one important aspect needs a special concern, which is that the electronic correlation in this atomically thick quasi-one dimensional GNS should be quite strong, especially for very narrow GNS. Thus, any small variation in the structure and/or environment will possibly result in an obvious discrepancy in the transport property between different GNSs. This issue may become harmful in large-scale integrated

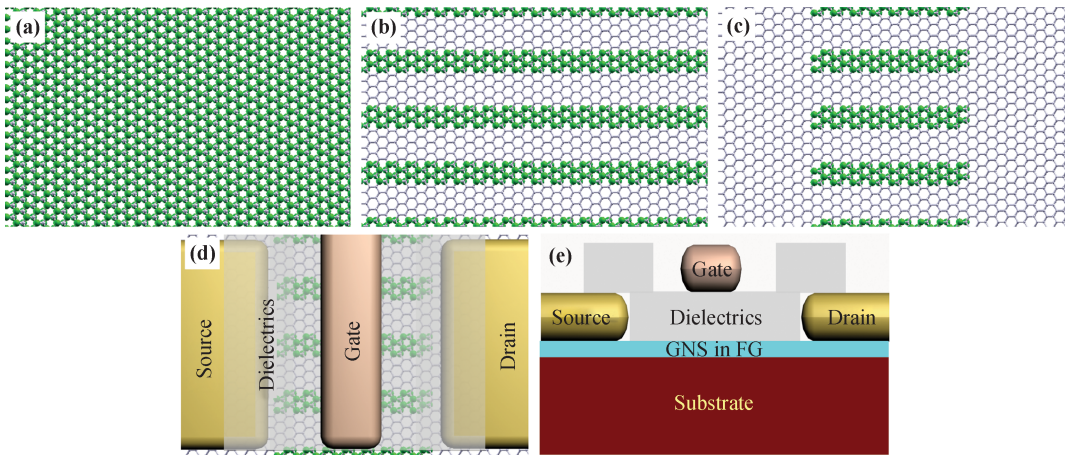

Fig. 2 The schematic drawings of **(a–d)** the fabrication steps of a GNS-FET, which consists of a couple of parallelized GNSs, and **(e)** the side view of a GNS-FET. The width of the GNSs should be sub-10-nm.

circuits if the unit device (GNS-FET) only consists of one GNS, because it is impossible that the structure and environment of different GNSs in the circuit be strictly all the same. This will introduce additional noise and limit the circuit performance. However, when parallelizing a couple of GNSs in an FET, the variation in the structure, environment, and then the transport property can be averaged out, and the noise will be lowered. The preparation steps for a GNS-FET consisting of a couple of GNSs are schematically shown in Figs. 2(a)–(e). This parallelization of several transport channels in an FET can be generalized to GNR-FET, too, which is schematically shown in Fig. 3. We could foresee that this parallelization approach can make the integrated FETs perform more uniformly and be immune to small structural and environmental perturbations, and should be preferred for high-quality graphene-based circuits.

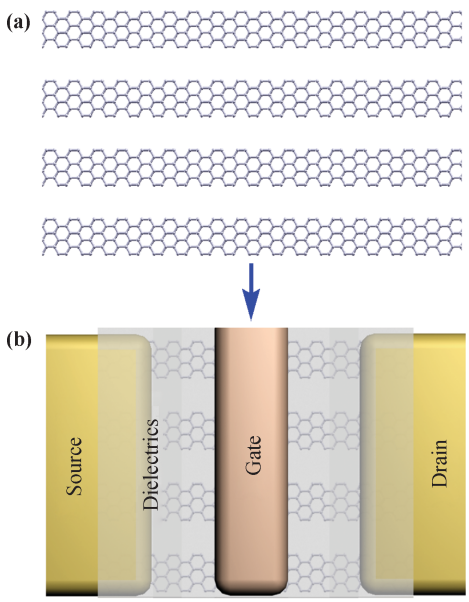

Fig. 3 Parallelizing a couple of GNRs in a GNR-FET could also make all the FETs in an integrated circuit perform more uniformly than those each consisting only of one GNR. The width of the GNRs should be sub-10-nm.

In summary, GNS sculptured in FG is a promising nanostructure for graphene transistor. Scanning-probe lithography can be used to obtain integrated, robust, and superior GNSs in substrate-supported FG. It is possible for GNS to overcome some obstacles currently facing the practical application of GNR. Parallelizing a couple of GNSs in a GNS-FET could make all the FETs in an integrated circuit perform uniformly and be immune to the structural and environmental perturbations, which also can be generalized to GNR-FET.

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