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Low Stress TSV Arrays for High-Density Interconnection

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ABSTRACT

In three-dimensional (3D) stacking, the thermal stress of through-silicon via (TSV) has a significant influence on chip performance and reliability, and this problem is exacerbated in high-density TSV arrays. In this study, a novel hollow tungsten TSV (W–TSV) is presented and developed. The hollow structure provides space for the release of thermal stress. Simulation results showed that the hollow W–TSV structure can release 60.3% of thermal stress within the top 2 μm from the surface, and thermal stress can be decreased to less than 20 MPa in the radial area of 3 μm. The ultra-high-density (1600 TSV·mm^{-2}) TSV array with a size of 640 × 512, a pitch of 25 μm, and an aspect ratio of 20.3 was fabricated, and the test results demonstrated that the proposed TSV has excellent electrical and reliability performances. The average resistance of the TSV was 1.21 Ω. The leakage current was 643 pA and the breakdown voltage was greater than 100 V. The resistance change is less than 2% after 100 temperature cycles from −40 to 125 °C. Raman spectroscopy showed that the maximum stress on the wafer surface caused by the hollow W–TSV was 31.02 MPa, which means that there was no keep-out zone (KOZ) caused by the TSV array. These results indicate that this structure has great potential for applications in large-array photodetectors and 3D integrated circuits.

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1. Introduction

Three-dimensional (3D) integration technology is expected to overcome the limitations of Moore's law owing to its advantages of low power consumption, small area, high performance, and high integration density [1]. Several key technologies such as through-silicon via (TSV), wafer thinning, and wafer/chip bonding [2] are required to achieve 3D integration. TSV is regarded as the core technology of 3D integration because it has the advantages of shortening the interconnection path and reducing the package size. At present, high-density TSV interconnection applications have attracted widespread attention, such as near-sensor and in-sensor computing [3], hybrid memory cubes [4], high-bandwidth memory (HBM) [5], complementary metal oxide semiconductor (CMOS) image sensors, cooled and uncooled focal plane arrays (FPAs), and active pixel sensors (APSs) [6]. High-density 3D interconnection requires high-density TSV arrays; however, certain problems limit the fabrication and use of high-density TSV arrays, the most important of which is the thermal stress of the TSV. TSV employ materials with different coefficients of thermal expansion (CTE) in the manufacturing process, in which thermal stress is unavoidable [7], thus resulting in a large thermal stress at the TSV–metal interface [8]. Thermal stress in a TSV can cause three problems. One is the difficulty in processing high-density TSV arrays because there are large temperature changes during processing, which may lead to bending or even destruction of the substrate. Second, it leads to reliability problems in the use of TSV, such as Cu extrusion [9], metal–SiO_2 or Si–SiO_2 interface delamination [10], Cu pumping [11], and chip cracking [12]. In most cases, the stress may not be sufficient to cause device failure but can lead to changes in transistor mobility and parameter shifts that affect transistor performance and tolerance [13]. In 3D integration, thermal stress has been reported to cause more severe reliability problems owing to high-power-density devices and high-density TSV [14]. Finally, to reduce the influence of thermal stress in a TSV, a certain keep-out zone (KOZ) is usually created around the TSV to prevent transistor placement [15]. Although this method reduces

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the adverse effects of thermal stress, it wastes substrate area, which is not conducive to improving chip integration.

To improve the thermodynamic reliability, reduce the thermal stress caused by TSV on substrates, and improve chip integration, methods to reduce the thermal stress of substrates around the TSV must be studied. One method is to use a hollow TSV to replace a solid TSV. Li et al. [16] fabricated a ring-shaped copper TSV (Cu–TSV) with an aspect ratio of 10:1 and filled the sidewall of the TSV with Cu metal with a thickness of 2 μm by sputtering, which can achieve lower thermal stress than the solid Cu–TSV. Khorramdel et al. [17] used inkjet printing technology to fill the hollow part of an annular TSV with a polymer, allowing under bump metallization (UBM), and solder balls to be directly fabricated on the bottom of the annular TSV to achieve a higher I/O density. Another method uses a soft polymer liner instead of SiO_2 as the dielectric layer. Thadesar and Bakir [18] proposed replacing the dielectric layer material with SU-8, which could not only reduce the influence of the stress introduced by the TSV on the silicon substrate, but also reduce the parasitic capacitance and improve the electrical performance. Similarly, Huang et al. [19] used an air gap to replace the traditional SiO_2 substrate as the insulating layer of a TSV. The air-gap structure provided free deformation space for the metal layer in the radial direction, alleviating the influence of thermal stress and reducing the stress to 80 MPa.

Another method involves filling the TSV with a conductive material that matches the CTE of Si. Tungsten has been investigated for TSV filling as its CTE (4.4 parts per million (ppm)·°C^{-1}) is close to that of silicon (2.3 ppm·°C^{-1}). Moreover, the chemical vapor deposition (CVD) method for filling tungsten has excellent step coverage and can fill TSV with a high depth-to-width ratio. Therefore, tungsten shows great potential as a TSV filler metal for large-scale high-density integration applications. Blasa et al. [20] fabricated a TSV with an aspect ratio of 12.5 for 3D stacking using W metal filling. Kikuchi et al. [21] successfully fabricated 47 μm deep solid W–TSV arrays for application in large-scale integration (LSI). Although the CTE of tungsten is closer to that of silicon, its hardness may lead to strain occurring primarily in the silicon substrate during thermal expansion, resulting in the silicon substrate being subjected to a greater degree of stress.

All of the aforementioned methods have contributed to reducing the TSV thermal stress. However, some methods are incompatible with CMOS processes, which limits their scope of application. Further research on low-stress TSV is required to satisfy the demands of high-density integration.

Based on the above-mentioned requirements, this study innovatively proposes a new type of hollow W–TSV with lower stress. The hollow structure inside the TSV was designed to provide a displacement space for thermal expansion so that the strain was mainly concentrated inside the TSV, thus reducing its impact on the silicon substrate. Through finite element analysis (FEA), the differences in the stress distribution between hollow W–TSV, solid Cu–TSV, and solid W–TSV were compared. Then, for the hollow TSV structure, a CMOS-compatible TSV-last process flow is developed, TSV of 5 μm diameter and 100 μm height is designed, and a 640 × 512 TSV array of 25 μm pitch, with 1600 TSV·mm^{-2} is successfully fabricated. Finally, electrical performance, reliability, and Raman spectroscopic stress tests were conducted to evaluate the performance of the sample.

2. Materials and methods

2.1. Model simulation and analysis

The schematic diagrams of the TSV models are shown in Figs. 1(a)–(c). The TSV was designed with smaller top and bottom dimensions and a larger middle dimension, as shown in Fig. 1(c). A larger middle section ensures that more metal is filled inside the hollow space, thus improving the performance of the electrical interconnect. To reduce the TSV thermal stress in the silicon substrate, W was selected as the filling metal in this study because its CTE is more similar to that of Si than that of Cu. Further, hollow W filling was performed to provide a thermal stress release space, and the port of the TSV was filled and closed with W, considering its compatibility with the traditional photoresist spin-coating and alignment process. Utilizing the very good step coverage characteristics of chemical vapor-deposited (CVD) W for high-aspect-ratio TSV, TSV are formed into structures with filled tops and bottoms, but with a vacuum region in between. This filling method not only has the advantage of low hollow stress, but is also suitable for traditional CMOS processes. The top diameter of the TSV hollow structure was designed to be 0.8 μm considering the electrical interconnection performance and thermal stress of the TSV (Section S1 in Appendix A). Two other structures were established to compare the thermal stresses. The solid Cu–TSV is shown in

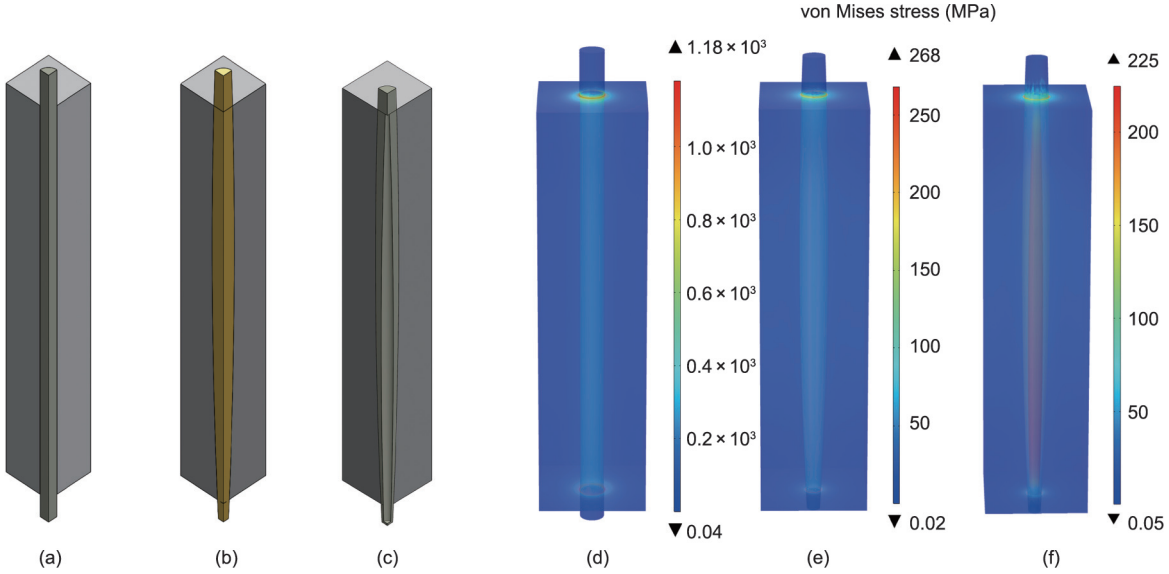

Fig. 1. (a–c) Schematic diagrams of the TSV models: (a) solid Cu–TSV, (b) solid W–TSV, and (c) hollow W–TSV. (d–f) Simulation diagrams of the von Mises stress distributions of the TSV: (d) solid Cu–TSV, (e) solid W–TSV, and (f) hollow W–TSV (the maximum stress is distributed inside the metal).

Fig. 1(a), and the solid W–TSV with a large diameter in the middle same as hollow W–TSV is shown in Fig. 1(b). This setup better demonstrates the ability of the hollow tungsten TSV to reduce thermal stress (Section S2 in Appendix A).

Three FEA models of the thermal stress were established using COMSOL software (COMSOL Inc., Sweden). The size of the TSV silicon substrate was 25 μm × 25 μm, the diameter of the top of the TSV was 5 μm, and its depth was 100 μm. 3D structural models were used, and the displacement around the silicon substrate along the direction perpendicular to the surface was fixed to simulate the constraints of the surrounding material. There are two options for physical modeling: isothermal and electrothermal. Considering that the TSVs play a role in signal transmission, the amount of Joule heat generated is limited (Section S3 in Appendix A). Joule heat can be further reduced by connecting multiple TSVs in parallel (Section S4 in Appendix A). Therefore, more attention should be paid to the thermal stress caused by the external environment of TSV, such as high temperatures involved in the process or temperature variations in the application environment. In this sense, isothermal conditions were adopted, and all materials were set to be elastic. The strain-free temperature was set to −200 °C (minimum temperature). To study the thermal stress change under a large temperature difference, the temperature is set to increase from −200 to 60 °C to simulate the thermal stress on the silicon substrates for the above-mentioned three structures. The material properties of the three structures are listed in Table 1.

Figs. 1(d)–(f) show the stress simulations of solid Cu–TSV, solid W–TSV, and hollow W–TSV at high temperatures. From Figs. 1(d) and (e), we can observe that the maximum stress of Cu can reach 1.18×10^3 MPa, whereas the maximum value for W is 268 MPa. This is mainly because the CTE of Cu is significantly larger than that of Si, whereas the CTE of W is similar to that of Si [22]. Therefore, when the temperature increased, Cu underwent greater deformation, resulting in increased stress. According to Figs. 1(e) and (f), the maximum stress in the hollow TSV can be further reduced to 225 MPa, which is a 16.04% reduction compared with the solid W–TSV. The maximum stress point of the hollow W–TSV occurred inside the metal, which is different from the metal–SiO_2 interface of the solid TSV. This hollow structure provides a space margin for the thermal expansion of W, such that when deformation occurs, W preferentially expands inward, and the stress point is concentrated on the inner side of the TSV metal, thus reducing the impact on the silicon substrate.

Table 1
Material properties.

Material	Young's modulus (GPa)	Poisson ratio	CTE (ppm·°C^{-1})
Silicon	130	0.28	2.3
Copper	110	0.35	17
Tungsten	400	0.28	4.4

To show the degree of reduction in the TSV effect on the silicon substrate for the hollow W–TSV, two-dimensional cross-sections of the von Mises stress distributions of the silicon substrates are shown in Fig. 2. The maximum von Mises stresses of the three silicon substrates were located at the top and bottom of the TSV, and the von Mises stress in the middle tended to decrease. As shown in Fig. 2(a), the maximum von Mises stress of the silicon substrate for the solid Cu–TSV is 1.16×10^3 MPa, and the von Mises stress at the middle position is 778.402 MPa showing a reduction of 32.90%. As shown in Fig. 2(b), the maximum von Mises stress on the silicon substrate for the solid W–TSV was 213 MPa, and the von Mises stress at the middle position was 122.353 MPa, representing a reduction of 42.56%. As shown in Fig. 2(c), the maximum von Mises stress of the silicon substrate for the hollow W–TSV is 166 MPa, and the von Mises stress at the middle position is 58.384 MPa, with a reduction of 64.84%. According to the simulation results, the thermal stress on the silicon substrate for the hollow W–TSV was significantly lower than those for the other two TSVs.

Fig. 3(a) shows the axial and radial directions of the TSV. Figs. 3(b) and (c) show the thermal stresses on the silicon substrate in the axial and radial directions. Along the axial direction in the range of 2 μm from the top, the stresses induced by the three TSV on the silicon substrate are reduced by 24.9%, 27.5%, and 60.3% (Fig. 3(b)). Evidently, the hollow W–TSV can better mitigate the thermal stress. The radial thermal stresses of the hollow W–TSV and the silicon substrate are shown in Fig. 3(c). The maximum thermal stress occurs inside the TSV at 221.4 MPa. Between the hollow W–TSV and Si, the stress decreased from 190.3 to 60.2 MPa. In the range of 3 μm, the thermal stress on the silicon surface is reduced to less than 20 MPa, which is significantly smaller than solid Cu–TSV and solid W–TSV (Section S5 in Appendix A).

2.2. Manufacturing process

The manufacturing process of the hollow W–TSV is illustrated in Fig. 4. This shows that the fabrication processes of the hollow

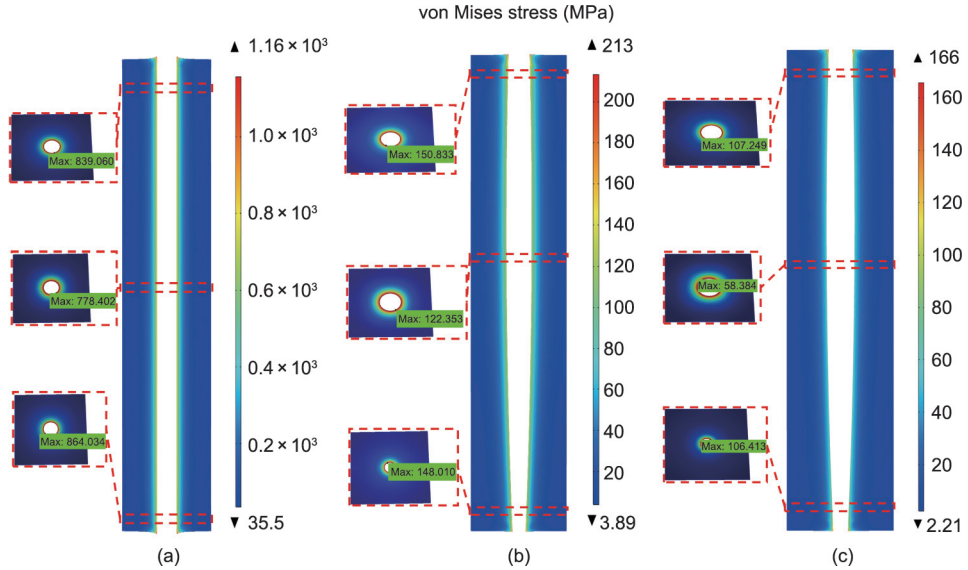

Fig. 2. Two-dimensional cross-sections of the von Mises stress distributions of silicon substrates: (a) solid Cu–TSV, (b) solid W–TSV, and (c) hollow W–TSV.

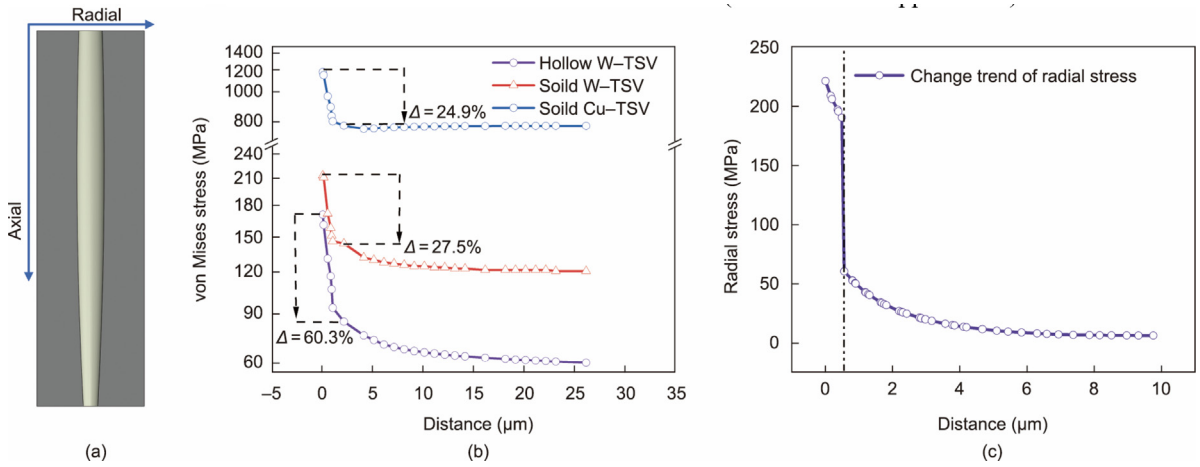

Fig. 3. (a) Axial and radial diagrams of TSV, (b) variation in the von Mises stress (Δ) of silicon substrates for the three TSV and (c) radial thermal stress curve of hollow W–TSV and silicon substrate.

W–TSV are the same as those of the traditional TSV fabrication processes, which is attributed to the hollow structure and optimized process. The process flow of a hollow TSV is described in detail below. Eight-inch 725 μm thick Si wafers are selected as the substrate. First, 4 μm thick layer of SiO_x is deposited as a hard mask. Subsequently, an array of 640 × 512 TSV was fabricated by dry etching. The hard mask layer was first etched, followed by the deep silicon via being etched by the Bosch process. We optimized the Bosch process by changing the ratio of etching gas SF_6 to passivation gas C_4F_8 during the cycle to achieve a hollow TSV topography with smaller top and bottom dimensions and a larger middle dimension. The next step is to deposit the dielectric layer material, which provides electrical isolation between the filling metal and Si substrate. The TSV is metal-filled after oxide layer deposition. Ti/TiN was deposited as the adhesion and barrier layers using CVD. CVD W is used to fill the TSV mainly because of the high step coverage required for a high-aspect-ratio TSV. Further, the CTE of W matches that of Si better than that of Cu. Subsequently, the front-side interconnection was made with AlCu metal to connect the TSV structure and form daisy chains for electrical performance testing. When the front-side interconnection is completed, processes such as front-side temporary bonding, back-side thinning, TSV via reveal, and metal interconnection are performed, all of which are consistent with the traditional processes. More manufacturing details can be found in Section S6 in Appendix A.

3. Results and discussion

3.1. Characterization of manufacturing

Fig. 5 shows a scanning electron microscopy (SEM; Hitachi, Japan) image and 3D X-ray rendering of the hollow W-TSV. The

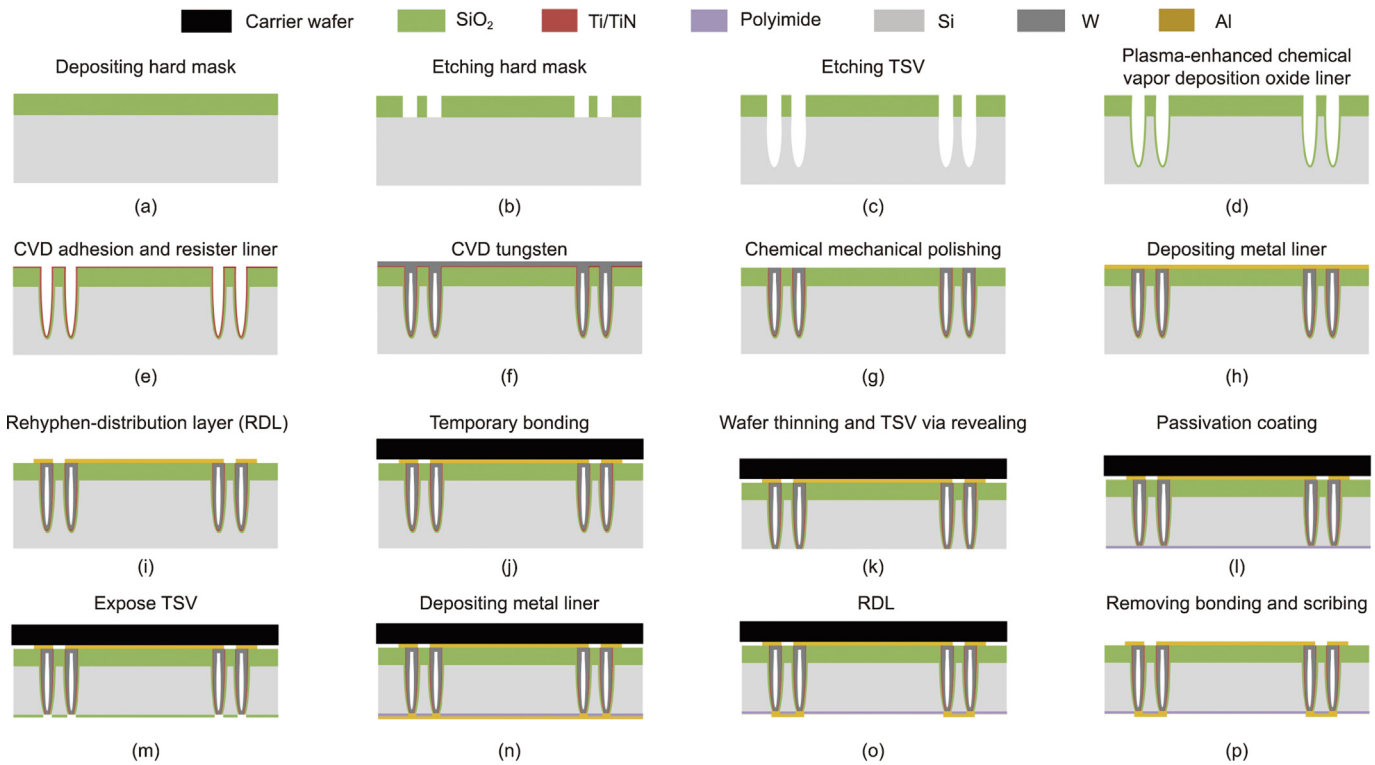

Fig. 4. Manufacturing processes of the hollow W–TSV.

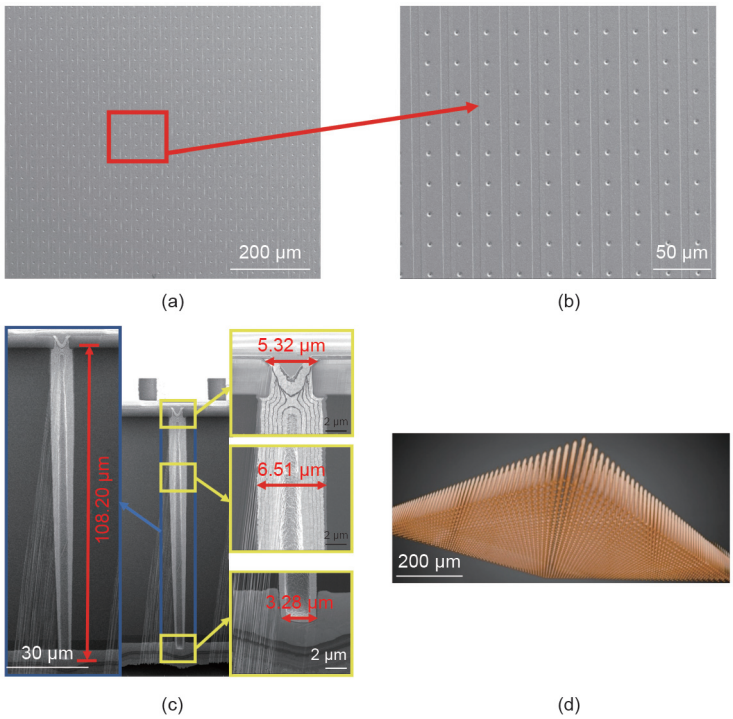

Fig. 5. (a) SEM image of TSV array. (b) Partially magnified SEM image of the TSV array. (c) SEM image of a single TSV and parameters of the TSV and (d) 3D X-ray rendering of the hollow W–TSV.

TSV parameters are listed in Table 2. The size of the TSV is 5.32 μm in top diameter and 108.2 μm in height, and it has an aspect ratio of 20.3. The TSV density reaches 1600 TSV·mm^{-2}. Most of the vacuum regions have a width of 2.39–2.42 μm. Because the top opening of the hollow TSV is filled during the metal filling, the subsequent process can still use the conventional spin-coating process, and there is no need to add a complex fabrication process. Figs. 5(a) and (b) show part of the TSV array, and the vias are arranged in an orderly manner. As shown in Fig. 5(c), the sidewalls of the TSV etched using the Bosch process were smooth, and the metal uniformly covered the sidewalls. The bottom of the TSV was completely covered by metal without voids, and there were no defects after thinning. This demonstrates the good reliability of the backside metallization process, which is fully applicable to the baseline process. Additional SEM images of the TSVs and resistance tests of the TSVs in different areas of the wafer show that the fabricated TSVs have very high yields (Section S7 in Appendix A). Therefore, the CMOS fabrication process can be used to fabricate hollow W–TSVs.

3.2. Electrical and reliability testing

The wafers were diced into 20 mm × 20 mm chips as test samples. To evaluate the electrical properties and reliability of the hollow W–TSV, a daisy-chain structure of 2000 TSV was fabricated around an array of 640 × 512 TSV. The properties were measured using a probe system (Cascade Microtech Summit 11000. Cascade Microtech, USA) and semiconductor parameter analyzer (Keithley 4200-SCS, Keithley Tektronix, USA).

Table 2
Hollow W–TSV parameters.

Dimension	Numerical value (μm)
Height	108.20
Hollow W–TSV top diameter	5.32
Hollow W–TSV middle diameter	6.51
Hollow W–TSV bottom diameter	3.28
Vacuum chamber height	105.40
Top sidewall metal thickness	4.06
Middle sidewall metal thickness	3.17
Bottom sidewall metal thickness	1.36

To eliminate the contact resistance of the probes, four-probe Kelvin structures were designed to test the TSV daisy chains. A total of 80 groups of 2000 TSV daisy chains were tested. Figs. 6(a) and (b) show the normal resistance distribution and resistance accumulation diagrams, respectively. Fig. 6(a) shows the normal distribution diagram, in which the resistance of a single TSV is between 1 and 1.35 Ω, and the average resistance value is approximately 1.21 Ω. The horizontal axis in Fig. 6(b) represents the unit resistance value, and the vertical axis represents the cumulative probability. According to the resistance accumulation diagram, the resistance values of the hollow W–TSV were low, and the resistance deviation was small, which can meet the requirements of electrical interconnections.

Figs. 6(c) and (d) show the TSV leakage current test diagram. Five different direct current (DC) voltages (5, 10, 15, 20, and 30 V) were applied to the two adjacent but unconnected TSVs. Fig. 6(c) shows that the leakage current stabilized within a very short time. Fig. 6(d) shows the cumulative leakage current at 5 V. The horizontal and vertical axes represent leakage current and cumulative probability, respectively. The leakage current did not change significantly; it was only 643 pA at 5 V and the variation range was very small.

Fig. 6(e) shows the breakdown voltage test with 5–100 V applied to the daisy chain of the two TSV. The current gradually increased as the voltage increased; however, no steep increase was observed. The current is only 25 nA at 100 V, no breakdown occurs between 0 and 100 V, and the breakdown voltage of the TSV exceeds 100 V. This demonstrates that the oxide layer of the TSV has good insulating properties.

To evaluate the reliability of the TSV, the samples were thermally cycled in accordance with JESD22–A104F [23]. The thermal cycle was performed using the high- and low-temperature test

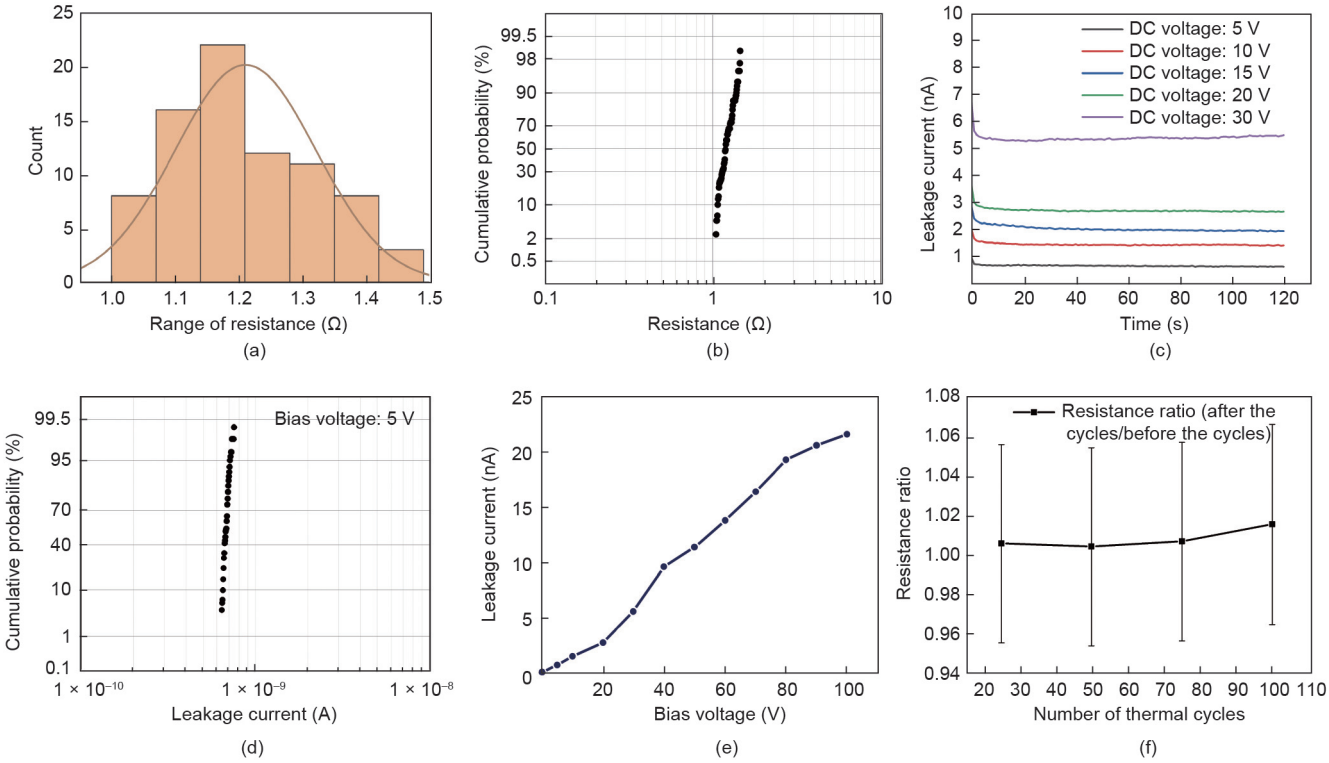

Fig. 6. Electrical performance testing of TSV arrays: (a) normal resistance distribution diagram, (b) resistance accumulation diagram, (c) leakage current test diagram at five different DC voltages (5, 10, 15, 20, and 30 V), (d) cumulative leakage current graph at 5 V, (e) breakdown voltage test with 5–100 V, and (f) thermal cycling test graph of TSV array from −40 to 125 °C.

chamber of the model PL-150. Each thermal cycle was of duration 30 min, with maximum and minimum temperatures of 125 and −40 °C, respectively. The resistance was measured every 25 cycles, and the average resistances after 25, 50, and 100 cycles are shown in Fig. 6(f). The average resistance value changed very little with increasing cycle number, with less than 2% change per chain. Therefore, it can be concluded that the TSV was sufficiently stable to adapt to changes in temperature.

The capacitance characteristics of the TSV were tested, and the results indicated that its capacitance was 468 fF at 1 MHz. This is due to the large depth and small pitch of the TSV, which inevitably leads to an increase in the insulating layer and substrate capacitances. In addition, the hollow structure contributes to a portion of the parasitic capacitance [24]. In subsequent studies, the parasitic capacitance can be further reduced by using a low-*k* material as the insulating layer or by reducing the size of the internal cavity of the TSV to realize high-performance and high-density 3D integration applications [25].

3.3. Stress measurement by Raman spectroscopy

To evaluate the stress distribution, the silicon surface was uncovered using a buffered oxide etchant and the near-surface stress was measured using micro-Raman spectroscopy. The measurement of local stress using Raman spectroscopy is based on the fact that the frequency shift of the Raman spectrum depends on the lattice shift of the silicon substrate under an external force or internal residual stress.

High-resolution X-ray diffraction can be used to calibrate the coefficient between the Raman frequency shift and stress on the silicon surface. The relationship between the stress and frequency shift follows a linear function [26]:

$$\sigma = -470\Delta\omega \quad (1)$$

where σ (MPa) is the sum of the radial and circumferential stresses in a cylindrical coordinate system and $\Delta\omega$ (cm^{-1}) is the Raman frequency shift.

The Raman frequency was measured using a Horiba Jobin Yvon HR800 spectrometer (French). The laser on the wafer surface scanned the silicon substrate with a length of approximately 20 μm between the two hollow W–TSVs, and the scanning step was 0.5 μm. Unstrained silicon has a reference frequency of approximately 520.7 cm^{-1}, depending on system calibration, and typically has a spectral resolution of ±0.02 cm^{-1}, corresponding to a stress resolution of approximately 10 MPa [27]. The near-surface stress distribution along the scanning path on a silicon substrate can be obtained using Eq. (1), as shown in Fig. 7. The position

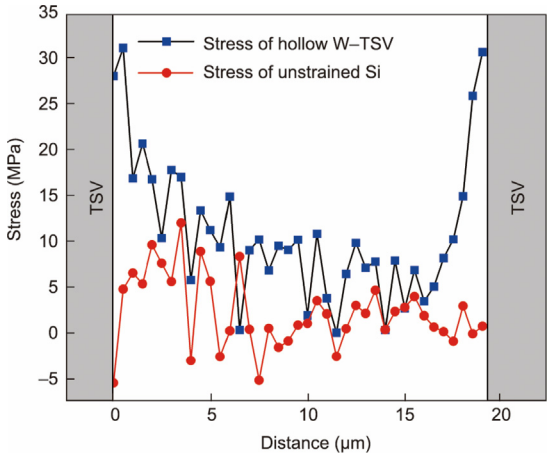

Fig. 7. The stress on the silicon substrate between two hollow W–TSV was measured by Raman spectroscopy.

Table 3
Various TSV structures to reduce thermal stress.

Institution	TSV type	Height (μm)	Aspect ratio	Center distance (μm)	Max stress (MPa)	Array size (numbers)
Freescale	Groove W [29]	160	2.7:1	230	800[#]	1 × 7
Nanyang Technological University	Low-*k* dielectric [34,35]	10.1	2.0:1	14.6	122 (25–200 °C)	10 × 10
NeRI	ATI [36]	20	2.0:1	40	150 (25–125 °C)	—
Tsinghua University	Air gap [19,37]	50	2.0:1	45	80[#]	11 × 11
NeRI	ATI [38]	40	4.0:1	20	300 (125–240 °C)	—
Tampere University of Technology	Annulus Cu [17]	305	1.5:1	500	—	8 × 4
IME	High-*k* dielectric [39]	42	11.0:1	—	220[#]	—
Xi'an Technological University	STI [40,41]	50	40.0:1	—	350 (25–275°C)	3 × 3
Our work	Hollow W	100	20.3:1	25	31.02[#]	640 × 512

[#] : This denotes the stress of the TSV silicon substrate measured using Raman spectroscopy, which contains the thermal stresses introduced by the process and residual stresses in the process, excluding thermal stresses. The other reported TSV stress results were obtained from simulations.

where the signal strength rapidly decreases represents the interface between the dielectric lining and silicon. The accuracy of the measured frequency shift decreased near the interface because the signal-to-noise ratio of the Raman spectrum decreased at lower relative intensities.

Between the two hollow W–TSV, all near-surface stresses in the silicon were tensile. The frequency at the center between two TSVs is 520.721 cm^{-1}, with a frequency shift of 0.021 cm^{-1}, corresponding to a stress of 9.87 MPa. The frequency fluctuations in the range of 0.008 to 0.038 cm^{-1} correspond to stresses of 3.76 to 17.86 MPa, which are mainly due to silicon surface defects and residual stress induced by chemical mechanical polishing (CMP) [28]. Therefore, the maximum frequency change is 0.066 cm^{-1}, corresponding to a stress of 31.02 MPa. The maximum stress appears in the range of 1 μm around the TSV, and the stress outside 2 μm is less than 20 MPa. This stress is lower than the thermal stresses reported in the literature [29–31]. It can also be observed from Fig. 7 that the surface stress curve of the unstrained Si fluctuates at approximately 0 MPa, which may be caused by system errors. Therefore, it can be speculated that the stress on the silicon surface caused by the hollow W–TSV was very small.

To facilitate comparison, the size of the KOZ region is used to describe the influence of thermal stress. KOZ is a region with a carrier mobility greater than 5% [32].

The relationship between carrier mobility and stress can be expressed as [33]:

$$\frac{\Delta\mu}{\mu} = \Pi \times \sigma \times \beta(\theta) \tag{2}$$

where σ is the TSV-induced stress, $\beta(\theta)$ is the orientation factor, θ is the angle between transistor channel and radial stress induced by TSV, and Π is the piezoresistive coefficient. μ and $\Delta\mu$ are the carrier mobility and the amount of stress-induced change in mobility, respectively.

According to Eq. (2), the maximum influence of the hollow W–TSV on the carrier mobility is 2.2%. Therefore, the hollow W–TSV has no KOZ region. The stress in the hollow W–TSV does not affect the carrier mobility of the surrounding devices and is thus beneficial for high-density integration applications.

3.4. Discussion

Table 3 lists the reported parameters for various TSV structures under reduced thermal stress. Our hollow W–TSV achieves an excellent combination of properties compared to the reported TSV. The structure achieved an aspect ratio of 20:1 with a diameter of only 5 μm. The pitch of the hollow W–TSV was 25 μm. The TSV array was of size 640 × 512, and the density was 1600 TSV·mm^{-2}. Furthermore, the maximum stress caused by the TSV is only 31.02 MPa, exhibiting the smallest TSV-induced stress reported to date. Therefore, our hollow W–TSV meets the standard for high-density integration and is characterized by low stress.

4. Conclusion

This paper proposes a hollow W–TSV with ultralow stress. A corresponding process was developed for fabricating the proposed hollow W–TSV. The top and bottom of the TSV were filled with W, for which spin coating could still be used rather than adding a complex process, and the vacuum area inside the TSV provided space for thermal stress release. Ultrahigh-density TSV chips (1600 TSV·mm^{-2}) with a TSV diameter of 5 μm, a pitch of 25 μm, and an array scale of 640 × 512 have been successfully fabricated through the collaborative innovation of structural design and processes. In addition, the chips were subjected to electrical, reliability, and Raman spectroscopic stress tests. The resistance of a single TSV is between 1 and 1.35 Ω, and the average resistance value is approximately 1.2 Ω, which meets the requirements of high-density integration. The leakage current was only 643 pA at 5 V and the variation was very small. The breakdown voltage exceeded 100 V, and the TSV exhibited good reliability. The resistivity changed by 2% after 100 temperature cycles from −40 to 125 °C, indicating that the structure of the TSV is sufficiently reliable. The wafer surface stress values measured using Raman spectroscopy are in the range of 3.76 to 31.02 MPa, which verifies that the proposed hollow TSV has extremely low stress and demonstrates that our TSV can be used for high-density 3D integration applications.

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Compliance with ethics guidelines

Binbin Jiao, Jingping Qiao, Shiqi Jia, Ruiwen Liu, Xueyong Wei, Shichang Yun, Yanmei Kong, Yuxin Ye, Xiangbin Du, Lihang Yu, and Bo Cong declare that they have no conflict of interest or financial conflicts to disclose.

Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.eng.2023.11.023.

References

[1] Shen WW, Chen KN. Three-dimensional integrated circuit (3D IC) key technology: through-silicon via (TSV). Nano Res Lett 2017;12(1):56.
[2] Zhu ZY, Yu M, Jin YF. Fabrication of integrated silicon PIN detector based on Al–Sn–Al bonding for ΔE–E telescope application. Microelectron Eng 2021;247:111599.
[3] Zhou FC, Chai Y. Near-sensor and in-sensor computing. Nat Electron 2020;3:664–71.
[4] Krihata T, Golz J, Wordeman M, Batra P, Maier GW, Robson N, et al. Three-dimensional dynamic random access memories using through-silicon-vias. IEEE J Emerg Sel Top Circuits Syst 2016;6(3):373–84.
[5] Park MJ, Lee J, Cho K, Park J, Moon J, Lee SH, et al. A 192-Gb 12-high 896-GB/s HBM3 DRAM with a TSV auto-calibration scheme and machine-learning-based layout optimization. IEEE J Solid-State Circuits 2023;58(1):256–69.
[6] Wang Z. 3-D integration and through-silicon vias in MEMS and microsensors. J Microelectromech Syst 2015;24(5):1211–44.
[7] Liu B, Satoh A, Tamahashi K, Sasajima Y, Onuki J. The protrusion behaviors in Cu–TSV during heating and cooling process. Trans Jpn Inst Electron Packag 2018;11:E17–014–1–8.
[8] Dou H, Yang M, Chen Y, Qiao Y. Analysis of the structure evolution and crack propagation of Cu-filled TSV after thermal shock test. In: Proceedings of the 2017 18th International Conference on Electronic Packaging Technology (ICEPT); 2017 Aug 16–19; Harbin, China. Piscataway: IEEE; 2017. p. 611–4.
[9] Kee SH, Kim WJ, Jung JP. Copper–silicon carbide composite plating for inhibiting the extrusion of through silicon via (TSV). Microelectron Eng 2019;214:5–14.
[10] Okoro C, Lau JW, Golshany F, Hummler K, Obeng YS. A detailed failure analysis examination of the effect of thermal cycling on Cu TSV reliability. IEEE Trans Electron Devices 2014;61(1):15–22.
[11] Beyne E. Reliable via-middle copper through-silicon via technology for 3-D integration. IEEE Trans Compon Packag Manuf Technol 2016;6(7):983–92.
[12] Lee K, Fukushima T, Tanaka T, Koyanagi M. Thermomechanical reliability challenges induced by high density Cu TSVs and metal micro-joining for 3-D ICs. In: Proceedings of the 2012 IEEE International Reliability Physics Symposium (IRPS); 2012 Apr 15–19; Anaheim, CA, USA. Piscataway: IEEE; 2012. p. 5F.2.1–2.4.
[13] Thompson SE, Sun G, Choi YS, Nishida T. Uniaxial-process-induced strained-Si: extending the CMOS roadmap. IEEE Trans Electron Devices 2006;53(5):1010–20.
[14] Huang C, Wu D, Wang Z. Thermal reliability tests of air-gap TSVs with combined air-SiO_2 liners. IEEE Trans Compon Packag Manuf Technol 2016;6(5):703–11.
[15] Wang F, Zhu Z, Yang Y, Yin X, Liu X, Ding R. An effective approach of reducing the keep-out-zone induced by coaxial through-silicon-via. IEEE Trans Electron Devices 2014;61(8):2928–34.
[16] Li C, Zou J, Liu S, Zheng H, Fei P. Study of annular copper-filled TSVs of sensor and interposer chips for 3-D integration. IEEE Trans Compon Packag Manuf Technol 2019;9(3):391–8.
[17] Khorramdel B, Liljeholm J, Laurila MM, Lammi T, Mårtensson G, Ebefors T, et al. Inkjet printing technology for increasing the I/O density of 3D TSV interposers. Microsyst Nanoeng 2017;3:17002.
[18] Thadesar PA, Bakir MS. Novel photo-defined polymer-enhanced through-silicon vias for silicon interposers. IEEE Trans Compon Packag Manuf Technol 2013;3(7):1130–7.
[19] Huang C, Wu K, Wang Z. Mechanical reliability testing of air-gap through-silicon vias. IEEE Trans Compon Packag Manuf Technol 2016;6(5):712–21.
[20] Blasa R, Mattis B, Martini D, Lanee S, Petteway C, Hong S, et al. High density backside tungsten TSV for 3D stacked ICs. In: Proceedings of the 2016 IEEE International 3D Systems Integration Conference (3DIC); 2016 Nov 08–11; San Francisco, CA, USA. Piscataway: IEEE; 2016. p. 1–4.
[21] Kikuchi H, Yamada Y, Mossad Ali A, Liang J, Fukushima T, Tanaka T, et al. Tungsten through-silicon via technology for three-dimensional LSIs. Jpn J Appl Phys 2008;47:2801.
[22] Pares G, Bresson N, Minoret S, Lapras V, Brianceau P, Sillon N, et al. Through silicon via technology using tungsten metallization. In: Proceedings of the 2011 IEEE International Conference on IC Design & Technology; 2011 May 2–4; Kaohsiung, China. Piscataway: IEEE; 2011. p. 1–4.
[23] Joint Electron Device Engineering Council (JEDEC). JESD22-A104F.01: Temperature cycling. JEDEC Standard. Arlington: JEDEC; 2020.
[24] Chandrakar M, Majumder MK. Performance analysis using air gap defected through silicon via: impact on crosstalk and power. IEEE Trans Compon Packag Manuf Technol 2022;12(11):1832–40.
[25] Liu F, Yu RR, Yong AM, Doyle JP, Wang X, Shi L, et al. A 300-mm wafer-level three-dimensional integration scheme using tungsten through-silicon via and hybrid Cu-adhesive bonding. In: Proceedings of the 2008 IEEE International Electron Devices Meeting; 2008 Dec 15–17; San Francisco, CA, USA. Piscataway: IEEE; 2008, p. 1–4.
[26] Hecker M, Zhu L, Georgi C, Zienert I, Rinderknecht J, Geisler H, et al. Analytics and metrology of strained silicon structures by Raman and nano-Raman spectroscopy. AIP Conf Proc 2007;931:435–44.
[27] Jian C, De Wolf I. Theoretical and experimental Raman spectroscopy study of mechanical stress induced by electronic packaging. IEEE Trans Compon Packag Manuf Technol 2005;28(3):484–92.
[28] Murugesan M, Kino H, Nohira H, Bea JC, Horibe A, Koyanagi M, et al. Wafer thinning, bonding, and interconnects induced local strain/stress in 3D-LSIs with fine-pitch high-density microbumps and through-Si vias. In: Proceedings of the 2010 International Electron Devices Meeting; 2010 Dec 6–8; San Francisco, CA, USA. Piscataway: IEEE; 2010. p. 2.3.1–4.
[29] Gambino J, Vanslette D, Webb B, Luce C, Ueda T, Ishigaki T, et al. Stress characterization of tungsten-filled through silicon via arrays using very high resolution multi-wavelength raman spectroscopy. ECS Trans 2011;35:105.
[30] Kwon WS, Alastair DT, Teo KH, Gao S, Ueda T, Ishigaki T, et al. Stress evolution in surrounding silicon of Cu-filled through-silicon via undergoing thermal annealing by multiwavelength micro-Raman spectroscopy. Appl Phys Lett 2011;98:232106.
[31] Trigg AD, Yu LH, Cheng CK, Kumar R, Kwong DL, Ueda T, et al. Three dimensional stress mapping of silicon surrounded by copper filled through silicon vias using polychromator-based multi-wavelength micro Raman spectroscopy. Appl Phys Express 2010;3:086601.
[32] Yin X, Zhu Z, Yang Y, Ding R. Metal proportion optimization of annular through-silicon via considering temperature and keep-out zone. IEEE Trans Compon Packag Manuf Technol 2015;5(8):1093–9.
[33] Wang F, Zhu Z, Yang Y, Liu X, Ding R. Analytical models for the thermal strain and stress induced by annular through-silicon-via (TSV). IEICE Electronics Expr 2013;10(20):20130666.
[34] Ghosh K, Zhang J, Zhang L, Dong Y, Li H, Tan CM, et al. Integration of low-κ dielectric liner in through silicon via and thermomechanical stress relief. Appl Phys Express 2012;5:126601.
[35] Lee S, Sugawara Y, Ito M, Kino H, Tanaka T, Fukushima T. TSV liner dielectric technology with spin-on low-k polymer. In: Proceedings of the 2018 International Conference on Electronics Packaging and iMAPS All Asia Conference (ICEP–IAAC); 2018 Apr 17–21; Mie, Japan. Piscataway: IEEE; 2018. p. 346–9.
[36] Wei F, Watanabe N, Shimamoto H, Kikuchi K, Aoyagi M. Analysis of thermal stress distribution for TSV with novel structure. In: Proceedings of the 2014 International 3D Systems Integration Conference (3DIC); 2014 Dec 1–3; Kinsdale, Ireland. Piscataway: IEEE; 2014. p. 1–4.
[37] Luo R, Ren K, Ma S, Yan J, Xia Y, Jin Y, et al. Fabrication and characterization of low stress Si interposer with air-gapped Si interconnection for hermetical system-in-package. In: Proceedings of the 2016 IEEE 66th Electronic Components and Technology Conference (ECTC); 2016 May 31–Jun 3; Las Vegas, NV, USA. Piscataway: IEEE; 2016. p. 1758–64.
[38] Feng W, Bui TT, Watanabe N, Shimamoto H, Aoyagi M, Kikuchi K. Fabrication and stress analysis of annular-trench-isolated TSV. Microelectron Reliab 2016;63:142–7.
[39] Chui K, Wang I T, Che F, Ji L, Yao Z. High aspect ratio (>10:1) via-middle TSV with high-k dielectric liner oxide. In: Proceedings of the 2019 IEEE 21st Electronics Packaging Technology Conference (EPTC); 2019 Dec 4–6; Singapore. Piscataway: IEEE; 2019. p. 721–4.
[40] Wang F, Qu X, Yu N. An effective method of reducing TSV thermal stress by STI. In: Proceedings of the 2019 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC); 2019 Jun 12–14; Xiamen, China. Piscataway: IEEE; 2019. p. 1–3.
[41] Liao S, Huang C, Zhang H, Liu S. Thermal stress study of 3D IC based on TSV and verification of thermal dissipation of STI. In: Proceedings of the 2021 22nd International Conference on Electronic Packaging Technology (ICEPT); 2021 Sep 14–17; Xiamen, China. Piscataway: IEEE; 2021. p. 1–5.