

Investigation of gate-all-around silicon nanowire transistors for ultimately scaled CMOS technology from top–down approach

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The gate-all-around (GAA) silicon nanowire transistor (SNWT) is considered one of the best candidates for ultimately scaled CMOS devices at the end of the technology roadmap. This paper reviews our recent work on the key issues regarding SNWTs from the top-down approach including process integration, carrier transport, and fluctuation and variability in these unique one-dimensional strongly-confined nanowire devices. A new process integration scheme for SNWTs is discussed, which features a fully-Si-bulk substrate, an epi-free process, a self-aligned structure and a large source/drain fan-out. The physical characteristics of the fabricated devices with 10-nm-diameter nanowires are further investigated. The carrier transport performance in SNWTs is experimentally estimated, with a modified extraction methodology which takes into account the impact of temperature dependence of parasitic source resistance. SNWTs with sub-40-nm gate lengths exhibit high ballistic efficiency at room temperature, indicating great potential for SNWTs as an alternative device structure for near-ballistic transport. For heat transfer in SNWTs, the self-heating effect is also characterized. However, due to the one-dimensional (1-D) nature of nanowires and increased phonon-boundary scattering in the GAA structure, the self-heating effect in SNWTs based on the bulk substrate is comparable or even a little bit worse than SOI devices, which may limit the ultimate performance of SNWT-based circuits and thus, special design consideration is expected. On the other hand, random variation has become a practical problem at nano-scale. The characteristic variability of SNWTs is experimentally studied in detail. The results of extracted variation sources indicate that, with suppressed random dopant fluctuations in the intrinsic channel, variations in radius and metal-gate work function of SNWTs dominate both the threshold voltage and on-current fluctuations. Comparing with conventional planar MOS devices, SNWT based SRAM cells exhibit better stability due to the superior electrostatic control in SNWTs.

Keywords silicon nanowire transistor (SNWT), gate-all-around (GAA), CMOS, top–down, quasi-ballistic transport, self-heating effect, variability

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1 Introduction

Si-based metal-oxide-semiconductor field-effect transistors (MOSFETs) are mainstream electronic devices in modern integrated circuits (ICs). For the last five decades, IC technology has been driven by device scaling to continually enhance performance, as well as to reduce cost and maintain low power consumption. However, in entering the sub-100-nm region, the performance gain of

Si MOSFETs has become increasingly difficult through traditional scaling. It is predicted by ITRS that the transistor gate length will ultimately reach about 6 nm at 14 nm technology node which is now considered as the end of the technology roadmap [1]. Many critical issues such as complex process integration, increased leakage current, short-channel effects, high-field effects, reliability, variability, noise, and parasitic effects may pose more obstructions for ultimately scaled devices. Therefore, a paradigm shift has been occurring in the industry and academe, where device structure and material innovation is becoming the primary enabler for performance enhancement in CMOS technology.

The gate-all-around (GAA) silicon nanowire transistor (SNWT) with the top-down approach has been attracting more and more attention as one of the most promising structures for the ultimately scaled device at the end of roadmap, due to its excellent gate control capability, improved transport property and feasible device design [2–8]. As shown in Fig. 1, this kind of device has a unique structural nature: for the nanowire channel, it is (quasi-) one-dimensional (1-D) and strongly confined; while within the surrounding gate-stack, it is three-dimensional and has multiple crystallographic interface orientations; for the source/drain region, there exists a sharp transition from a large source/drain to the nanowire. Therefore, the above mentioned critical issues may be even more complicated, which would give rise to new challenges in the device engineering of SNWTs. On the other hand, these nanowire devices provide a unique opportunity to investigate the device physics in quasi-one dimensions. We have investigated the parasitic effects [9], reliability [10, 11] and noise characteristics [12–14] in SNWTs. This paper will focus on experimental investigations of some other key issues of SNWTs, including process integration, carrier transport and variability.

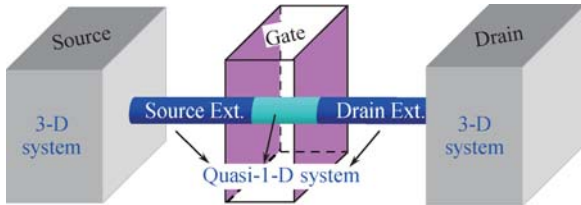


Fig. 1 Schematic view of a gate-all-around silicon nanowire transistor.

2 Process integration of GAA SNWT based on a fully-Si-bulk substrate

Although bottom-up methods using CVD, MBE and other processes to grow semiconductor nanowires have been extensively studied, there still exist some problems such as orientation control, process repeatability and effective nanowire integration. Recently, the SNWTs fabricated by the top-down process have been given more

attention due to the CMOS technology compatibility [2–7]. Some methods were put forward based on the bulk Si substrate with a selective epitaxial process and sacrificial SiGe layers for nanowire structure release [4, 5]. The SOI substrate is another choice with Si/SiGe multi-layer stack structure fabricated for final nanowire channel formation [3, 6].

We have proposed a new process integration method based on fully-Si-bulk substrate for the fabrication of GAA SNWTs with both deep S/D regions and large fan-out through epi-free fully compatible CMOS technology [8]. As shown in Fig. 2, without the SiGe layers in the S/D region, the device can be immune to the degraded strain in NMOSFET, as well as to the low heat conductivity of SiGe. Also, the device can also avoid high parasitic source/drain (S/D) resistance resulting from ultra-thin films and worse heat dissipation capability of the SOI substrate.

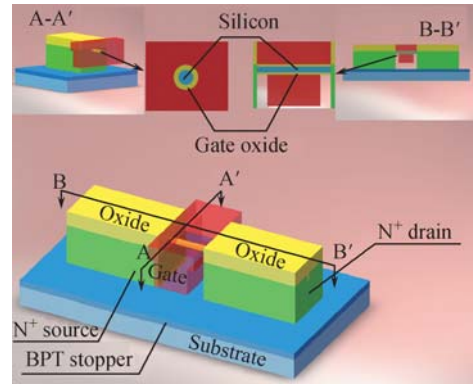


Fig. 2 Schematic view of the proposed SNWT in this work from bird's eye.

Figure 3 gives the main fabrication process flow. After the isolation process, the nitride was patterned as the fin hard mask, followed by the oxide spacer formation and S/D implantation. After gate trench etching, the grooves were formed and the wide fan-out S/D regions were defined. Then, the nitride spacer was formed to protect the fin channel. ICP etching was used to expose the region beneath the channel and the silicon under the channel was removed by the subsequent isotropic silicon etching. The bridge-like channel was thus formed. Then the high dose of substrate implantation was performed to suppress the bottom parasitic transistor (BPT) and achieve a better isolation of the bottom gate. After the nitride hard mask removal, the sacrificial oxidation was used to thin the silicon channel. It can be seen from SEM images that the shape of the nanowire can change from triangular to cylindrical with the diameter decreasing (the figures are not given here). Then the gate oxide was grown and the gate trench was filled by poly-silicon in a self-aligned manner. Finally, back-end steps including contact-hole etching, metal deposition, and metal patterning steps were performed to complete the process.

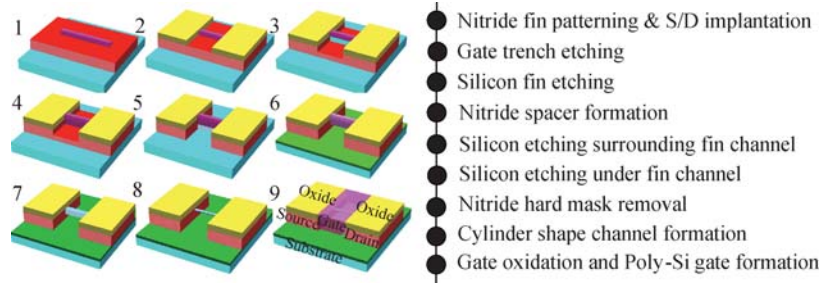


Fig. 3 Fabrication process flow without epitaxy technology.

Figure 4 shows the cross-sectional and tilted top view SEM images of the fabricated SNWT with a 10 nm diameter after poly-Si deposition without the sacrificial oxide removal. Multi-wire SNWTs for high performance applications can also be achieved in this work [8].

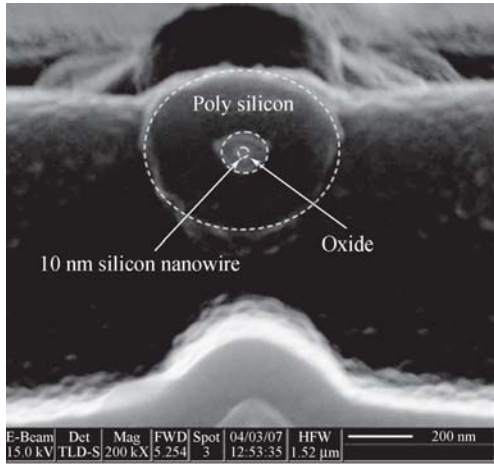


Fig. 4 SEM micrographs of the SNWT with 10 nm diameter after poly-Si deposition without sacrificial oxide removal.

The obtained large fan-out and deep junction of the source/drain region can decrease the parasitic resistance. Since the source/drain regions connect with the bulk substrate, the heat can be spread quickly throughout the substrate and self-heating effects can be effectively suppressed. Figure 5 and Fig. 6 show measured I_d - V_g and I_d - V_d characteristics of the fabricated SNWT with a sin-

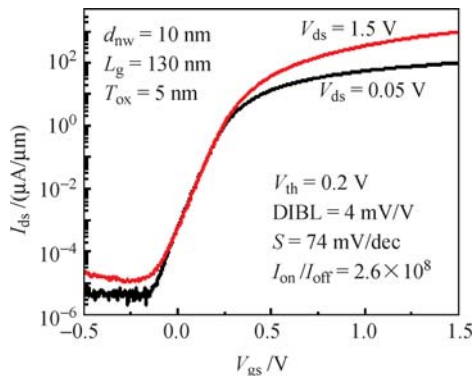


Fig. 5 Measured I_d - V_g characteristics of fabricated bulk SNWT with single wire.

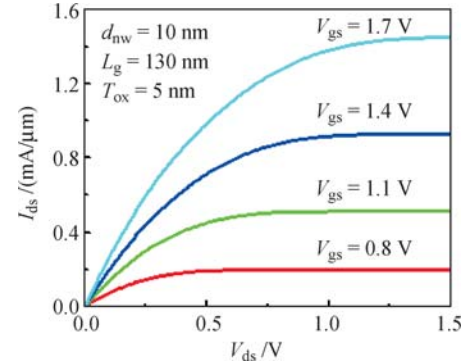


Fig. 6 Measured I_d - V_d characteristics of fabricated SNWT with single wire.

gle wire. Despite the 5 nm gate oxide, 1.04 mA/ μ m driving currents and 12 pA/ μ m leakage current of n-SNWT are achieved. The record I_{on}/I_{off} ratio of 2.6×10^8 is obtained, mainly resulting from better control of the silicon wire interface, better heat dissipation and low S/D resistance in this structure. Further measured results of the SNWT with 4 nanowires shows a driving current about 4 times larger compared with the device with a single wire, which shows the feasibility and potentials of SNWTs for high performance applications.

3 Experimental studies on carrier transport and self-heating effect in SNWTs

3.1 Carrier transport behavior of short-channel SNWTs

The gate-all-around silicon nanowire transistors with quasi-1-D channel structures may exhibit some new transport features. The simulation results have shown that SNWTs may approach ballistic transport [15], and Coulomb oscillations at ultra-low temperature have also been experimentally reported [16]. However, the quasi-ballistic transport in SNWTs has rarely been characterized and experimentally discussed.

Based on the Lundstrom theory [17], a kind of temperature dependent I - V technique was developed to extract the channel backscattering factor r_{sat} and ballistic efficiency B_{sat} [18]. This extraction method makes an

assumption that the temperature dependence of the device's source resistance R_S is negligible, which is appropriate for planar devices with channel and source/drain (S/D) regions in similar dimensions. However, for the quasi-1-D nanowire structures, which are connected to 3-D S/D regions in an abrupt way, the temperature dependence of R_S cannot be ignored. This is due to the fact that the quantum contact resistance R_Q , which is a part of R_S and originates from the interface between the 3-D S/D regions and quasi-1-D quantum-wire of the S/D-extension regions, is sensitive to temperature [19] and may be further enhanced by some parasitic effects. Moreover, the collection efficiency of the channel has exponential dependence on the carrier mean free path which is also temperature dependent. A modified experimental extraction methodology for SNWTs is proposed [20], as shown in Fig. 7, and the temperature dependence of source resistance has been included through the β factor.

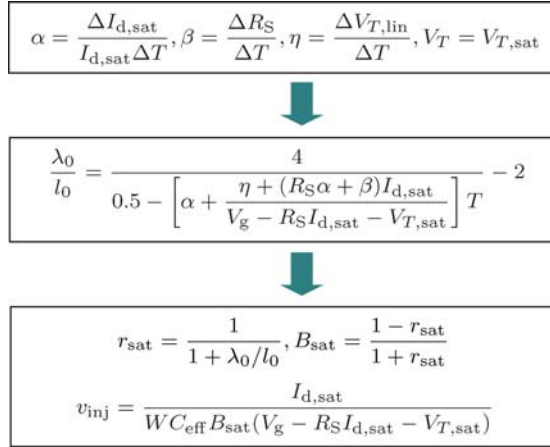


Fig. 7 Flow chart of the methodology used to extract backscattering parameters for SNWTs.

The SNWTs used in this section are Twin Silicon Nanowire MOSFETs with a gate-all-around structure whose channel consists of two nanowires. The fabrication details were given in early work [4]. The temperature dependence of R_S in the SNWT is measured around 300 K and found to be $\beta = 41 \text{ } \Omega/\text{K}$. This value is relatively large compared to planar devices (β of planar double-gate MOSFETs with $W = 10 \text{ } \mu\text{m}$ is $0.02 \text{ } \Omega/\text{K}$, which can be ignored).

Figure 8 compares the extracted r_{sat} for SNWTs with or without the correction. It can be explicitly seen that severe overestimation occurs if the temperature dependence of R_S is neglected. Figure 9 further plots the extracted B_{sat} of the SNWTs compared with conventional planar bulk MOSFETs [21] as functions of the gate length. The ballistic efficiency exhibits remarkable increase especially when SNWTs enter the sub-40-nm region, which is earlier than bulk MOSFETs, due to the larger low-field mean-free-path in SNWTs. The extracted carrier injection velocity v_{inj} at the source is al-

most unchanged due to the thermal injection limit, which indicates the possibility of further performance enhancement with some strain engineering.

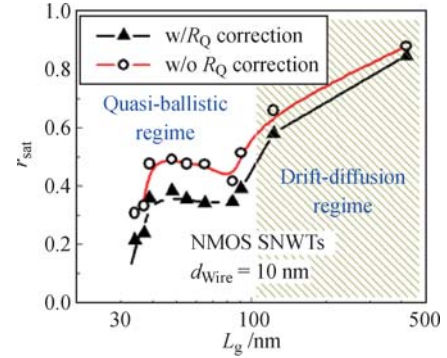


Fig. 8 The extracted r_{sat} in n-channel SNWTs with and without the temperature dependence of R_S .

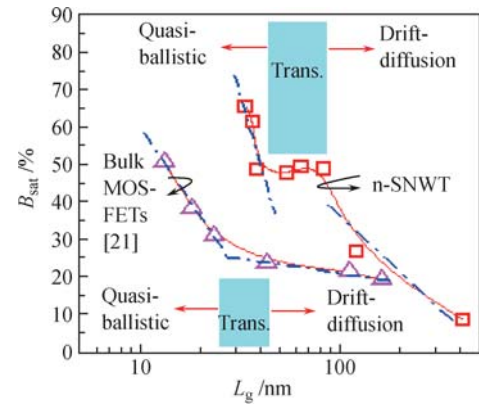


Fig. 9 Extracted B_{sat} of the fabricated SNWTs and bulk MOSFETs.

Figure 10 shows the ballistic limit, the Shur's model predictions as well as experimental data of n-channel and p-channel SNWTs. The apparent mobility in short-channel SNWTs is extracted using the Y-function technique [22, 23]. It is clearly seen that GAA SNWTs approach the ballistic limit as the gate length shrinks. Due to the combination of 1-D nanowires and gate-all-around structures, the nano-scaled GAA NWFET can be one of the promising structures that provide the possibility of near-ballistic MOSFET from the top-down approach.

3.2 Self-heating effects in SNWTs

With the device size scaling and circuit density increasing, self-heating effect (SHE) attracts growing concerns. In order to avoid the additional influence of SOI or SiGe on self-heating, the SNWTs for self-heating effect investigation are fabricated on fully-Si-bulk substrate, with the process details discussed in Section 2 [8]. A multi-finger structure is used, with the G-S-G test structure for high-frequency measurements [24]. The AC conductance technique [25] is adopted to characterize SHE and to extract the thermal resistance (R_{th}) of SNWTs, with g_{ds} measured at high frequencies.

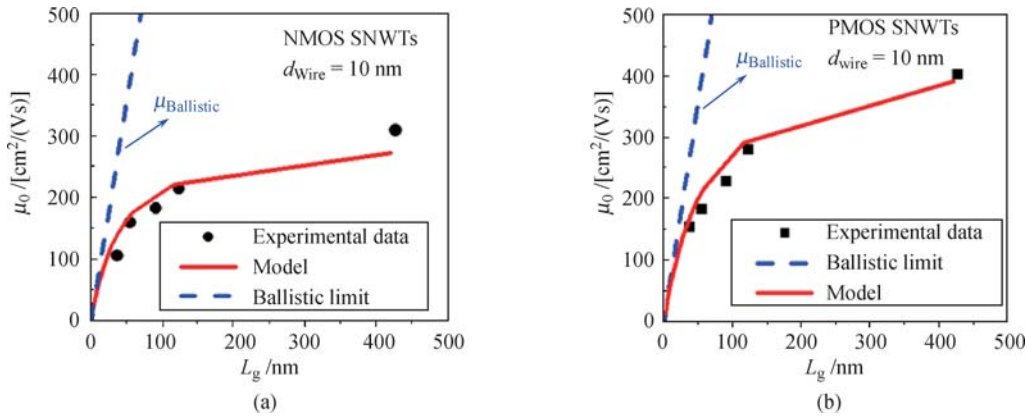


Fig. 10 Comparison among the ballistic limit, model predictions and the experimental data of (a) n-channel SNWTs and (b) p-channel SNWTs.

Figure 11 plots measured AC and DC output characteristics of the fabricated SNWTs. It can be observed that the DC current of SNWTs is evidently reduced at high drain biases, exhibiting severe SHE. Figure 12 compares the extracted thermal resistance (R_{th}) of SNWTs, SOI devices [26–29] and bulk MOSFETs [26]. It can be seen that the thermal conductivity of SNWTs is comparable or even a little bit worse than SOI devices, although the SNWTs are fabricated on fully-Si-bulk substrates. The heat transport in the nanowire channel is in quasi-one dimension, and there are limited modes for heat dissipation in SNWTs resulting from the strong-confined nanowire. Moreover, additional contact thermal resistance can occur in the SNWTs at the abrupt interface between the 1-D-nanowire channel and the 3-D S/D region, which does not exist in the planar devices. Also, the GAA architecture of SNWTs with a high surface to volume ratio may induce additional phonon-boundary scattering, which is worse than double-gate or tri-gate structures.

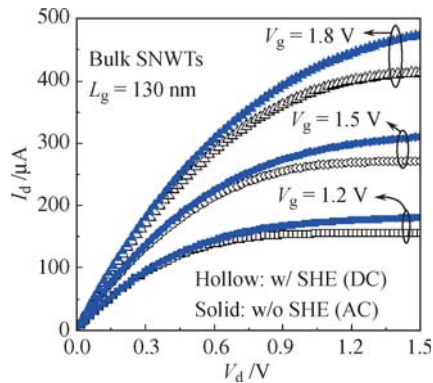


Fig. 11 Measured DC and AC output characteristics of the SNWT.

Taking into account the influence of the self-heating effect, the temperature of the drain side will be higher than the source side, which can lead to increased negative current flux from the drain according to the Lundstrom theory [17]. Thus, the ultimate performance of SNWT-based circuits may be intrinsically limited by self-

heating effects, and special design considerations are expected, such as new thermal-aware design methodology for SNWT circuits.

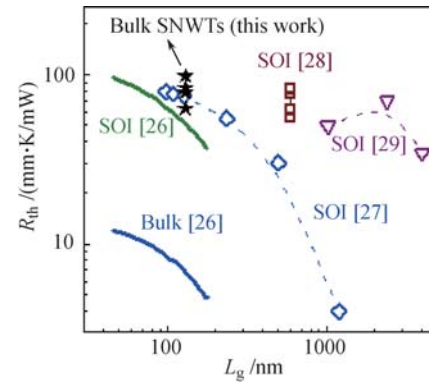


Fig. 12 Comparison of thermal resistance of the SNWT, SOI and bulk devices.

4 Experimental study on characteristic variability in SNWTs

One of the potential bottlenecks for the future application of SNWT-based circuits is variability due to the ultra-scaled dimension of nanowires. The variation sources and their impacts in SNWTs may be quite different from conventional planar devices due to the unique device structure and electrical properties. We have experimentally investigated this issue [30]. The characterization is performed on GAA twin Si nanowire transistors with gate lengths varying from 37 nm to 427 nm.

Variation sources in SNWTs are schematically shown in Fig. 13 and experimentally extracted, including effective channel length (L) variation, metal-gate work-function (WF) variation, nanowire radius (R) variation, apparent mobility variation (μ_0) under the quasi-ballistic framework, variation of mobility attenuation factors (θ_1 and θ_2), and line-edge-roughness (LER). It is worth noticing that as illustrated in the figure, the L variation consists of two parts, one being the variation of the gate line pattern due to lithography and etching fluctuations,

and the other can be ascribed to the variation of dopant diffusion in the source/drain extension regions [30].

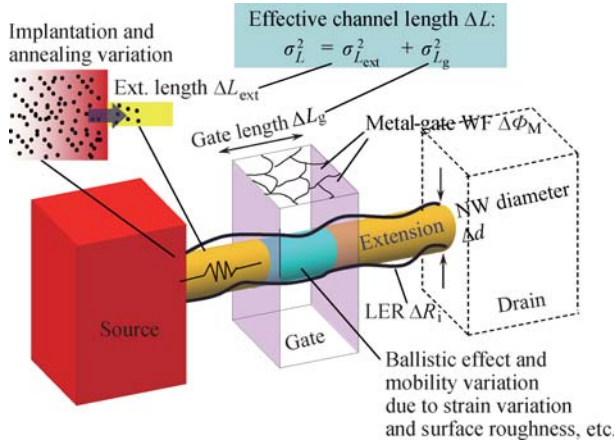


Fig. 13 Schematic view of 3-D SNWT and various fluctuation sources in SNWTs.

The V_{th} and I_{on} variations were measured in SNWTs with different L_g , as shown Fig. 14 and Fig. 15, which illustrate that the agreement of measured and simulated data in terms of both V_{th} and ON current variations are simultaneous. Figure 16 further presents the contributions of different variation sources in SNWTs as a function of the gate length L_g . For $\sigma_{V_{th}}$, with the absence of random dopant fluctuation (RDF), R variation is dominant due to the impact of strong quantum confinement in ultra-scaled nanowire channels. Gate WF variation is another main contributor especially with L_g scaling. This can be attributed to the variation of crystal orientation and grain size of the metal-gate, especially when the area of the gate region is comparable to the grain size [31, 32], especially with L_g scaling. For $\sigma_{I_{on}}$, R also variation dominates due to the modification of effective gate capacitance and V_{th} by quantum effects. Considering the remarkable impacts of R variation on both V_{th} and ON current variation, suppression of R variation is of primary importance for SNWTs. Besides, transport-related variation (μ_0 , θ_1 and θ_2) also contribute to the ON current variation.

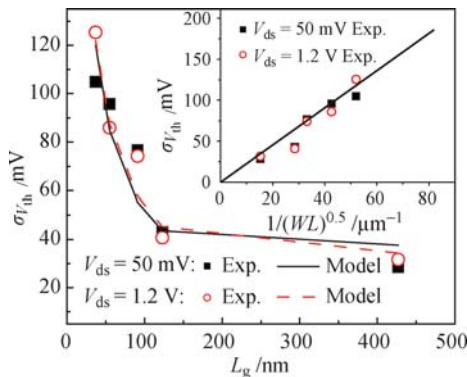


Fig. 14 Measured gate length dependence of $\sigma_{V_{th}}$ and the results by Monte Carlo calculation of SNWTs.

We also evaluated the SRAM noise margin variations

for a SNWT based circuit, compared with conventional planar bulk MOSFETs, as shown in Fig. 17 as an example. The SNWT based SRAM cell is more stable than the planar MOSFET based SRAM cell due to the superior electrostatic control and thus better immunity of surface potential variations in SNWTs. Consequently, SNWTs are good candidates for future SRAM cell applications from the perspective of variation suppression.

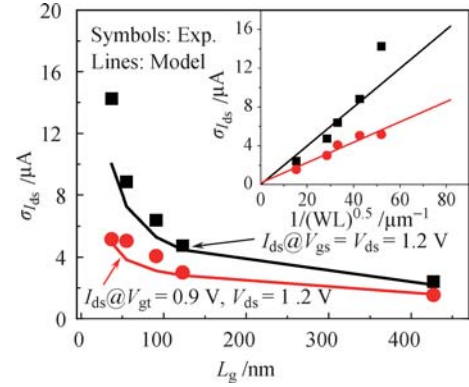


Fig. 15 Measured and calculated gate length dependence of I_{ds} variation at $V_{gs} = V_{ds} = 1.2$ V and $V_{gt} = 0.9$ V, $V_{ds} = 1.2$ V.

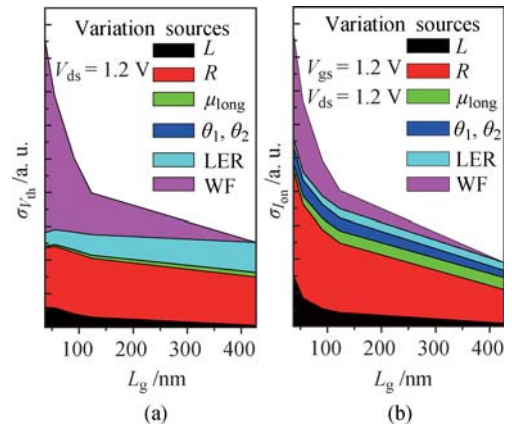


Fig. 16 Contributions of different fluctuation sources in SNWTs to V_{th} (a) and I_{on} (b) variations.

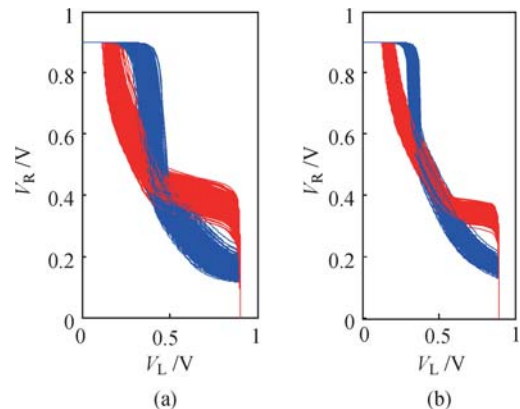


Fig. 17 SRAM butterfly curves based on planar MOSFETs (a) and SNWTs (b) with $L_g = 32$ nm.

5 Conclusion

This paper discusses some critical issues in GAA SNWTs for ultimate CMOS applications, with focuses on the compatible process integration scheme and physical characterization. With a kind of epi-free new top-down process approach, SNWTs with a 10-nm diameter, large S/D fanout, and a self-aligned structure have been successfully fabricated, featuring record high on-off current ratio. The transport behavior of the SNWTs is experimentally investigated, with an improved extraction methodology of the typical transport parameters proposed. Short-channel SNWTs exhibit great potential for near-ballistic transport. However, due to the 1-D nature of the nanowire and increased phonon-boundary scattering in the GAA structure, the experimentally extracted SHE parameters in the SNWTs based on bulk substrate are comparable or even a little bit worse than SOI devices. Special design consideration for the self-heating effect is expected to enhance the performance of SNWT-based circuits. The characteristic variability in GAA SNWTs is also experimentally studied. The measured results show that with suppressed random dopant fluctuations (RDF) in the intrinsic channel, variations in radius (R) and metal-gate work function (WF) of SNWTs dominate both the threshold voltage and on-current fluctuations. The influence of the SNWT variation sources on SRAM performance is estimated and compared with planar devices, which indicates that the SNWT based SRAM cell is more stable than planar MOSFET based SRAMs due to better electrostatic control.

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References

1. Available: <http://public.itrs.net/>
2. F. L. Yang, D. H. Lee, H. Y. Chen, C. Y. Chang, S. D. Liu, C. C. Huang, T. X. Chung, H. W. Chen, C. C. Huang, Y. H. Liu, C. C. Wu, C. C. Chen, S. C. Chen, Y. T. Chen, Y. H. Chen, C. J. Chen, B. W. Chan, P. F. Hsu, J. H. Shieh, H. J. Tao, Y. C. Yeo, Y. Li, J. W. Lee, P. Chen, M. S. Liang, and C. Hu, in: *VLSI Symp. Tech. Dig.*, 2004: 196
3. N. Singh, F. Y. Lim, W. W. Fang, S. C. Rustagi, L. K. Bera, A. Agarwal, C. H. Tung, K. M. Hoe, S. R. Omampuliyur, D. Tripathi, A. O. Adeyeye, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, in: *IEDM Tech. Dig.*, 2006: 547
4. S. D. Suk, S. Y. Lee, S. M. Kim, E. J. Yoon, M. S. Kim, M. Li, C. W. Oh, K. H. Yeo, S. H. Kim, D. S. Shin, K. H. Lee, H. S. Park, J. N. Han, C. J. Park, J. B. Park, D. W. Kim, D. Park, and B. I. Ryu, in: *IEDM Tech. Dig.*, 2005: 735
5. K. H. Yeo, S. D. Suk, M. Li, Y. Yeoh, K. H. Cho, K. H. Hong, S. Yun, M. S. Lee, N. Cho, K. Lee, D. Hwang, B. Par, D. W. Kim, D. Park, and B. Ryu, in: *IEDM Tech. Dig.*, 2006: 735
6. N. Singh, A. Agarwal, L. K. Bera, T. Y. Liow, R. Yang, S. C. Rustagi, C. H. Tung, R. Kumar, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, *IEEE Electron Device Lett.*, 2006, 27: 383
7. Y. Jiang, T. Y. Liow, N. Singh, et al., in: *VLSI Symp. Tech. Dig.*, 2008: 27
8. Y. Tian, R. Huang, Y. Wang, J. Zhuge, R. Wang, J. Liu, X. Zhang, and Y. Wang, in: *IEDM Tech. Dig.*, 2007: 895
9. J. Zhuge, R. Wang, R. Huang, X. Zhang, and Y. Wang, *IEEE Trans. Electron Devices*, 2008, 55: 2142
10. R. Wang, R. Huang, D. W. Kim, Y. He, Z. Wang, G. Jia, D. Park, and Y. Wang, in: *IEDM Tech. Dig.*, 2007: 821
11. L. Zhang, R. Wang, J. Zhuge, R. Huang, D. W. Kim, D. Park, and Y. Wang, in: *IEDM Tech. Dig.*, 2008: 123
12. J. Zhuge, R. Wang, R. Huang, Y. Tian, L. Zhang, X. Zhang, D. W. Kim, D. Park, and Y. Wang, *IEEE Electron Device Lett.*, 2009, 30: 57
13. J. Zhuge, L. Zhang, R. Wang, R. Huang, D. W. Kim, D. Park, and Y. Wang, *Appl. Phys. Lett.*, 2009, 94: 083503
14. L. Zhang, J. Zhuge, R. Wang, R. Huang, C. Liu, D. Wu, Z. Kang, D. W. Kim, D. Park, and Y. Wang, in: *VLSI Symp. Tech. Dig.*, 2009: 46
15. J. Wang, E. Polizzi, and M. Lundstrom, in: *IEDM Tech. Dig.*, 2003: 695
16. K. H. Cho, S. D. Suk, Y. Y. Yeoh, M. Li, K. H. Yeo, D. W. Kim, S. W. Hwang, D. Park, and B. I. Ryu, in: *IEDM Tech. Dig.*, 2006: 543
17. M. S. Lundstrom and J. Guo, *Nanoscale Transistors: Device Physics, Modeling and Simulation*, New York: Springer, 2006
18. M. J. Chen, H. T. Huang, K. C. Huang, P. N. Chen, C. S. Chang, and C. H. Diaz, in: *IEDM Tech. Dig.*, 2002: 39
19. S. Datta, *Electronic Transport in Mesoscopic Systems*, London: Cambridge University Press, 1997
20. R. Wang, H. Liu, R. Huang, J. Zhuge, L. Zhang, D. W. Kim, X. Zhang, D. Park, and Y. Wang, *IEEE Trans. Electron Devices*, 2008, 55: 2960
21. J. Jeon, J. Lee, J. Kim, C. H. Park, et al., in: *Symposium on VLSI Technology*, 2009: 48
22. G. Ghibaudo, *Electron. Lett.*, 1988, 24: 543
23. A. Cros, K. Romanjek, D. Fleury, S. Harrison, R. Cerutti, P. Coronel, B. Dumont, A. Pouydebasque, R. Wacquez, B. Duriez, R. Gwoziecki, F. Boeuf, H. Brut, G. Ghibaudo, and T. Skotnicki, in: *IEDM Tech. Dig.*, 2006: 663
24. R. Wang, J. Zhuge, R. Huang, D. W. Kim, D. Park, and Y. Wang, *IEEE Electron Device Lett.*, 2009, 30: 559
25. R. Agaiby, A. O'Neill, S. Olsen, G. Eneman, P. Verheyen, R. Loo, and C. Claeys, in: *Proc. ESSDERC*, 2006: 97
26. K. Etesam-Yazdani, R. Hussin, and M. Asheghi, in: *Proc.*

- ITHERM, 2006: 1257
27. G. Guegan , R. Gwoziecki, O. Gonnard, G. Gouget, C. Raynaud, M. Casse, and S. Deleonibus, in: Proc. Mater. Res. Soc. Symp., 2006, 913: 0913-D03-02
28. W. Jin, W. Liu, S. K. H. Fung, P. C. H. Chan, and C. Hu, IEEE Trans. Electron Devices, 2001, 48: 730
29. B. M. Tenbroek, G. Whiting, M. S. L. Lee, and C. F. Edwards, IEEE Trans. Electron Devices, 1996, 43: 2240
30. J. Zhuge, R. Wang, R. Huang, J. Zou, X. Huang, D. W. Kim, X. Zhang, D. Park, and Y. Wang, in: IEDM Tech. Dig., 2009: 61
31. K. Ohmori, T. Matsuki, D. Ishikawa, T. Morooka, T. Aminaka, Y. Sugita, T. Chikyow, K. Shiraishi, Y. Nara, and K. Yamada, in: IEDM Tech. Dig., 2008: 409
32. H. Dadgour, K. Endo, V. De, and K. Banerjee, in: IEDM Tech. Dig., 2008: 705