



LK–MVS joint modeling for NCFET circuit robustness and digital decoder delay variation analysis



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ABSTRACT

Timing variability induced by device manufacturing fluctuations has become a pervasive and critical challenge for low-voltage logic circuits, which severely impairs the timing margin and operational accuracy of core peripheral circuits such as decoders. In sub-1-V low-voltage applications, gate-level delay discretization in decoders will be magnified into wordline arrival-time mismatches, posing insurmountable obstacles to the realization of low-power and high-reliability integrated systems. To address this issue, this paper proposes a closed-loop paradigm integrating device modeling-circuit implementation-robustness evaluation-feedback design for ferroelectric negative-capacitance field-effect transistors (NCFETs) in low-voltage logic applications. First, under a strict charge-conservation framework, the Landau-Khalatnikov (LK) ferroelectric dynamics is coupled with the MIT virtual-source (MVS) channel conduction model to construct a simulation program with integrated circuit emphasis (SPICE)-compatible compact model for NCFETs that can characterize device-to-device (DTD) variations. Second, DTD variations are explicitly introduced to simulate process fluctuations in ferroelectric layer thickness (t_{FE}), and the resulting statistical perturbations are propagated from the device level to the gate-level 2-to-4 decoder circuit. Finally, with the 2-to-4 decoder as a case study, the propagation delays of all output signals are quantified, and a “DTD-centric” feedback path aimed at design-window convergence is formulated. The results show that within a process window of approximately $t_{FE} \approx 10$ nm, the proposed model successfully reproduces experimentally comparable I - V characteristics; the NCFET-based 2-to-4 decoder maintains correct functionality under low voltage drain V_{DD} , and the coefficient of variation (C_V) of its propagation delay is controlled within 3%–7%, exhibiting a substantial design optimization window for low-voltage logic design.

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1 Introduction

In the post-Moore era, non-volatile memories (NVMs) oriented toward “compute-in-memory/near-memory computing” have become the key pathway for improving system-level energy efficiency. Among them, resistive RAM (RRAM), magnetic RAM (MRAM), phase-change RAM (PCRAM), ferroelectric capacitor-based RAM (FeRAM), and ferroelectric field-effect transistors (FeFETs) represent the most prominent device families, and exhibit “application-specific partitioning” at the circuit level of on-chip cache, embedded memory, and analog/digital neuromorphic accelerators [1–3]. In near-memory or compute-in-memory accelerators, peripheral row/column selection circuits directly determine array-level throughput and energy efficiency, where the decoder acts as the “first hop” linking higher-level control logic to the wordline/bitline array. When the operating voltage drops to sub-1 V or even lower, the drive strength and timing margin of conventional CMOS decoding chains shrink rapidly; any gate-level delay discretization can be magnified into wordline arrival-time mismatches (skew), thereby affecting array access windows and computational accuracy. Therefore, establishing a quantifiable delay-distribution model along the decoder’s critical path and identifying dominant sources of variation become essential prerequisites for achieving low-voltage, low-energy solutions. Negative-capacitance field-effect transistors (NCFETs), by introducing a ferroelectric layer into the gate stack, exhibit an apparent subthreshold swing below 60 mV/dec and an “intrinsic voltage amplification” effect, making them naturally suited for low-voltage decoding applications. A 2-to-4 decoder built with NCFETs typically consists of input inverter stages, AND/OR logic stages (functionally equivalent to two-level combinational logic), and an output buffer stage. Theoretically, it can reduce propagation delay and gate count at the same low voltage drain V_{DD} , thereby achieving a smaller energy-delay product. However, the electrical advantages of NCFETs are highly dependent on the ferroelectric layer thickness t_{FE} and polarization dynamics. Statistical fluctuations in t_{FE} can induce significant variability in the effective threshold voltage, gate capacitance distribution, and transconductance gain. Meanwhile, intrinsic polarization relaxation/switching introduces history-dependent and transient nonlinear behavior. These factors collectively affect the gate-level high-to-low/low-to-high propagation delays (t_{pHL}/t_{pLH}), rise/fall times, and overshoot/ringing characteristics, which ultimately manifest as the arrival-time distribution and inter-output skew across the cascaded decoding path.

With the discovery of HfO_2 -based ferroelectrics, CMOS-compatible materials such as HZO have provided a practical route for implementing NCFETs on silicon platforms, including demonstrations of hysteresis-free/low-subthreshold swing (SS) operation and 14-nm process integration [4]. Meanwhile, physical constraints such as stabilization mechanisms and speed limits [5] impose new co-design requirements for circuit and system levels. Recent studies on nano-scale semiconductor devices have provided important references for the variation-aware design and compact modeling of NCFETs. Fuad et al. [6] conducted a comprehensive performance analysis of CMOS and carbon nanotube field-effect transistor (CNTFET)-based 8T SRAM cells, revealing the significant impact of device-level variations and environmental factors on circuit timing characteristics and verifying the superiority of novel nano-devices in low-power and high-speed applications. Also, they proposed a high-efficiency modeling technique for single-walled CNTFETs, analyzing the impact of dielectric materials and oxide thickness on device conductance under ballistic transport conditions, and enriching the technical system of nano-device compact modeling considering structural and material variations [7]. Besides, the further research supplemented the correlation research between device-level physical parameter fluctuations and circuit-level performance degradation in nano-scale devices, emphasizing the necessity of establishing a full-chain analysis framework from device modeling to circuit performance evaluation [8].

Although recent studies have made progress in NCFET compact modeling and circuit-level evaluation [9,10], and relevant nano-device research has provided valuable methodological references, the research on NCFETs still faces a prominent research gap that the existing NCFET compact models have not yet constructed a unified framework that connects statistical device-to-device (DTD) variations to circuit-level delay distributions, while also providing a practical feedback mechanism for design and technology co-optimization (DTCO). Current models mostly focus on the characterization of single NCFET device electrical characteristics, lacking the ability to quantitatively propagate device-level DTD variations to the circuit level, and cannot map circuit-level performance evaluation results back to device-level parameter

optimization, which severely restricts the practical application of NCFETs in high-robustness low-voltage logic circuits.

In this work, we establish a closed-loop analytical framework that connects device variability of NCFETs to circuit-level robustness, thus tightly coupling NCFET device behavior with the performance and stability of logic circuits. The main contributions of this work are as follows: i) development of an Landau-Khalatnikov-MIT virtual-source (LK-MVS) joint compact model for NCFETs in the post-Moore era, which can accurately characterize DTD variations induced by ferroelectric layer thickness fluctuations; ii) statistical analysis of threshold voltage and on-state current variations under DTD perturbations, along with their propagation into 2-to-4 decoder circuits and quantitative characterization of circuit-level delay distribution; iii) proposal of a feedback design strategy based on the propagation delay distribution of decoders, realizing the closed-loop co-optimization of NCFET device design and logic circuit design.

2 Modeling framework

To accurately capture the physical behavior of NCFETs, we begin with the device structure illustrated in Fig. 1(a), which shows a typical ferroelectric transistor with a metal-ferroelectric-insulator-semiconductor (MFIS) gate stack. The corresponding capacitive network is depicted in Fig. 1(b), highlighting the series connection between the ferroelectric capacitance (C_{FE}) and the underlying MOS capacitance (C_{MOS}).

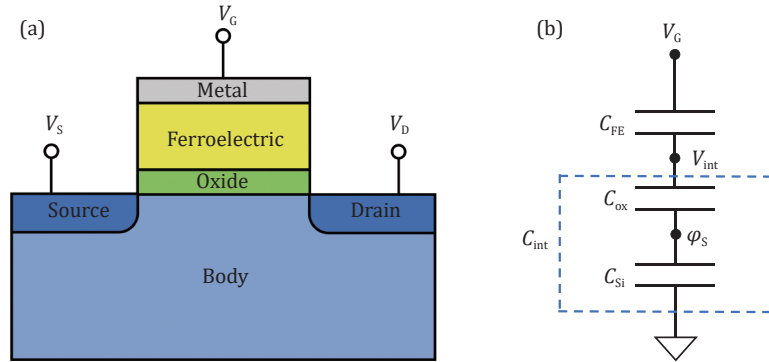


Fig. 1. Structure and electrostatic capacitive model of a FeFET device: (a) schematic diagram of a ferroelectric transistor and (b) schematic diagram of the capacitor stack.

To clarify the implementation logic and ensure the reproducibility of the proposed methodology, Fig. 2 is first presented to systematically illustrate the full-chain process from device modeling to the circuit-level delay analysis. The flowchart integrates key links including experimental data preprocessing, model calibration, variation mapping, circuit implementation, and statistical analysis, with explicit labeling of input/output parameters and core operation tools for each step. This visual framework establishes a clear connection between discrete technical modules, facilitating readers to replicate the entire simulation process.

2.1 LK model

For the physical characteristics of negative-capacitance transistors, the LK equation is employed to describe the dynamics of ferroelectric

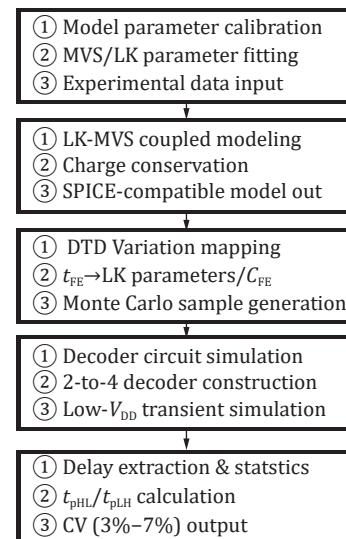


Fig. 2. Flowchart of the LK-MVS joint modeling and simulation workflow.

polarization P , where the Gibbs free energy function G includes terms $\alpha P^2 + \beta P^4 + \gamma P^6$ and the external electric-field coupling term. Through the MFIS series constraint, the ferroelectric terminal voltage is mapped to the gate terminal, jointly determining with the external load the “stabilizable negative-slope” region [11]. In combination with the energy landscape shown in Fig. 3 (0 V/forward bias/reverse bias), the target window for hysteresis-free operation is used to physically bound $(\alpha, \beta, \gamma, t_{\text{FE}})$. The following equations are given, where G is Gibbs free-energy density of ferroelectric HZO thin-film, α, β , and γ are temperature-dependent Landau phenomenological coefficients for ferroelectric polarization-energy polynomials, P is the polarization charge density inside the ferroelectric layer, E is the average electric-field intensity across the ferroelectric film, ρ is the dynamic viscosity coefficient related to polarization switching speed in the LK equation, V_G is the total gate voltage applied across the MFIS gate stack, A is gate-overlap area of the underlying MOS transistor, C_{MOS} is the equivalent capacitance contributed by the MOS-channel part, and C_{FE} is the thesmall-signal equivalent capacitance extracted from ferroelectric film.

- i) Gibbs free energy: $G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP$
- ii) LK dynamic equation: $\rho \frac{dP}{dt} = -(2\alpha P + 4\beta P^3 + 6\gamma P^5 - E)$
- iii) Steady-state E–P relation: $E = 2\alpha P + 4\beta P^3 + 6\gamma P^5$
- iv) Negative-capacitance condition: $\frac{dP}{dE} = \frac{1}{2\alpha + 12\beta P^2 + 30\gamma P^4} < 0$
- v) MFIS voltage constraint: $V_G = t_{\text{FE}} (2\alpha P + 4\beta P^3 + 6\gamma P^5) + \frac{AP}{C_{\text{MOS}}}$
- vi) Stability condition: $\frac{1}{C_{\text{FE}}} + \frac{1}{C_{\text{MOS}}} > 0$

2.2 MVS model

The MVS model describes current conduction starting from the “barrier-top/virtual-source injection” mechanism, using a small set of physically interpretable parameters to cover the subthreshold, velocity-saturation, and strong-inversion regimes simultaneously. Its core idea is that the I – V behavior is determined by the carrier velocity and effective channel charge at the virtual source, while accounting for vertical-field-induced mobility degradation, drain-induced barrier lowering (DIBL), body effect, and temperature dependence. This yields a unified expression that remains robust from long-channel to deep-submicron devices. Furthermore, an intrinsic charge model is embedded to ensure charge conservation and consistency. Compared with “fully physical” models, the MVS model requires fewer parameters that can be directly extracted from experimental curves, making it suitable for use as the MOS core in series with the LK block in NCFET modeling.

$$I_{\text{DS}} = W Q_{\text{inv}}^{\text{vs}} F_{\text{sat}} V_{\text{inj}} \{1 - \exp[-V_{\text{DS}}/(\xi V_{\text{DSsat}})]\} / \{1 + [V_{\text{DS}}/(E_c L_g)]\}$$

where I_{DS} is drain-to-source channel current of NCFET, W represents the transistor channel width, $Q_{\text{inv}}^{\text{vs}}$ is the inversion-layer charge density under velocity-saturation condition, F_{sat} is the saturation correction factor for carrier transport, V_{inj} represents the virtual-source carrier injection velocity, ξ represents the MVS model fitting coefficient, V_{DS} is the drain-source bias voltage, V_{DSsat} is the saturation drain-source voltage, E_c is the critical saturation electric field of silicon channel, and L_g is the physical gate length of transistor.

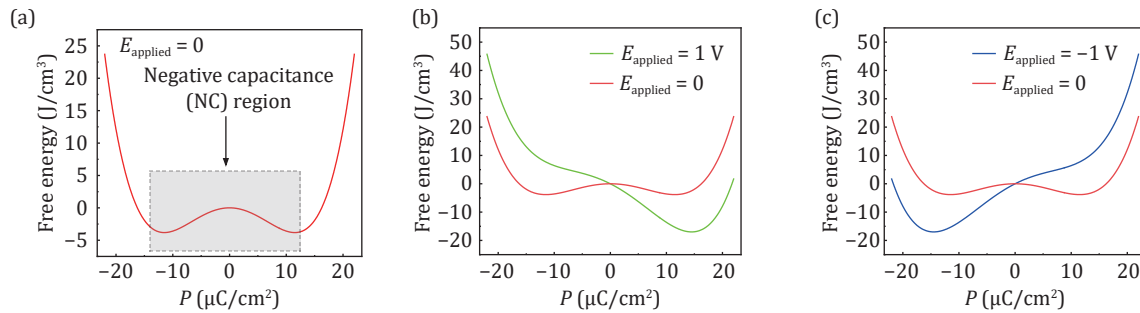


Fig. 3. Gibbs free energy curves of the ferroelectric material under different applied voltages: (a) 0, (b) 1 V, and (c) –1 V.

2.3 NCFET SPICE model

At the SPICE implementation level, the LK block and the MVS channel are coupled through charge conservation, with port configurations identical to those of conventional MOSFETs, facilitating direct gate-level circuit reuse [12,13]. The overall structure of the LK-MVS joint model is illustrated in Fig. 4(a), where the LK ferroelectric block and the MVS channel are coupled via charge conservation. Figs. 4(b) and (c) further demonstrate the numerical computations of charge conservation and surface potential, respectively, ensuring model consistency in both DC and transient simulations.

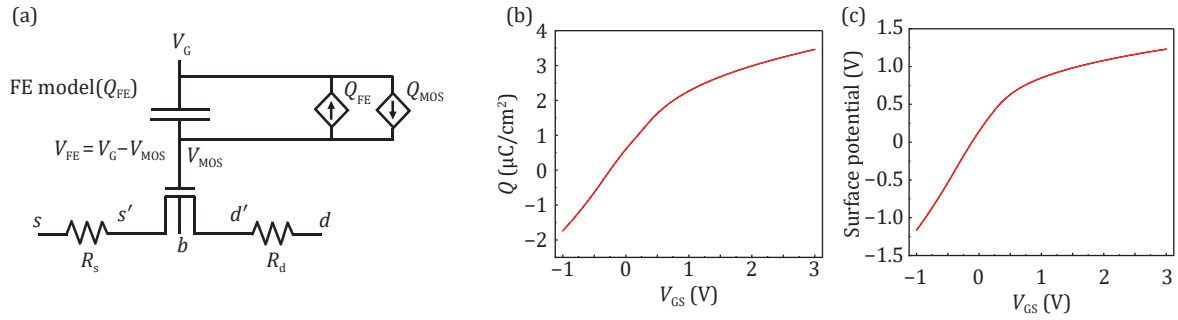


Fig. 4. Proposed LK-MVS joint model for FeFET simulation: (a) schematic of the LK-MVS joint model, (b) numerical computation of charge conservation, and (c) numerical computation of surface potential.

In Cadence Spectre/APS, we implement a “charge-conserving coupling of LK ferroelectric layer + MVS MOS core”. Tables 1 and 2 summarize calibration results and statistical priors for both LK and MVS components. The LK part, implemented as a Verilog-A equivalent circuit, captures ferroelectric hysteresis and dynamic response. Additional custom ports ensure charge continuity, and Spectre’s differential-algebraic equation solver guarantees iterative convergence for both DC and transient analyses. The MVS model, as a short-channel-friendly, current/charge-consistent compact model, handles channel transport and charge calculation. Together, the two models form an MFIS/NCFET gate stack representing the causal chain of intrinsic-gain-to-gate-drive-to-transient-waveform. Numerical stability is ensured via charge-conserving modeling, convergence/step-size control, and conservative/gear settings [14–18].

After completing a two-step calibration (“non-ferroelectric to ferroelectric integration”), statistical fluctuations of t_{FE} are introduced as Monte Carlo perturbation sources, mapped onto LK parameters, and equivalent small-signal capacitances. The resulting distributions of gate-level propagation delay, rise/fall times, and overshoot/ringing metrics are obtained. Subsequently, the same subcircuit is used to construct a 2-to-4 decoder, where the propagation delay of four output signals with respect to input transitions is evaluated under a target load. A full-

Table 1
Parameters of the LK model.

Parameter	Value
α	-1.8×10^{11}
β	-5.8×10^{22}
γ	0.0
ρ	9
t_{FE}	10 nm

Table 2
Fitted parameters of the MVS model(a).

Parameters	Value
Version	1.01
Channel width W	0.0001 cm
Gate length L_g	3.2×10^{-6} cm
Gate length offset/bias δ_{Lg}	9×10^{-7} cm
Gate capacitance C_g	2.57×10^{-6} F/cm ²
Oxide capacitance C_{ox}	0.0013 cm
Mobility degradation coefficient δ	0.0883
Subthreshold swing factor at zero bias n_0	1.5513
Source series resistance R_{s0}	62.1604 $\Omega \cdot \mu\text{m}$
Drain series resistance R_{d0}	100 $\Omega \cdot \mu\text{m}$
Inner fringe capacitance C_{if}	1×10^{-12} F/cm
Critical velocity for velocity saturation V_{xo}	1.5355×10^{-7} cm/s
Effective carrier mobility μ	185.49 cm ² /(V·s)
Velocity saturation fitting parameter β	1.8
Junction temperature T_{jun}	298 K

chain Monte Carlo simulation using identical samples then quantifies the timing and waveform variability along the “ t_{FE} →gate-level→decoder-link” path. The proposed methodology is supported by: i) the equivalent-circuit formulation and numerical implementation of the LK model, ii) circuit-level portability of the MVS virtual-source model, iii) Spectre’s support for conservative Verilog-A systems and charge conservation, and iv) established engineering practices for 2-to-4 decoder delay evaluation.

To quantitatively characterize the impact of process-induced fluctuations on NCFET performance, this section explicitly defines the mapping logic between ferroelectric layer thickness (t_{FE}) variation and key LK model parameters, as well as the equivalent small-signal capacitance. This mapping is derived from the physical properties of ferroelectric materials and ensures the statistical consistency between device-level variations and circuit-level responses.

The variation of t_{FE} during the atomic layer deposition (ALD) process is assumed to follow a normal distribution, which is consistent with the statistical characteristics of nanoscale semiconductor manufacturing fluctuations. The nominal value of t_{FE} is set to 10 nm, with a fluctuation range of $\pm 20\%$ to cover typical process variations. The mathematical expression of t_{FE} variation is given by

$$t_{FE} = t_{FE,nominal}(1 + \Delta t)$$

where $t_{FE,nominal} = 10$ nm is the nominal ferroelectric layer thickness, and Δt follows a normal distribution $\Delta t \sim N(0, \sigma^2)$ with $\sigma = 0.1$. This parameter setting ensures that the 3σ range of t_{FE} variation covers the $\pm 20\%$ fluctuation (i.e., $t_{FE} \in [8 \text{ nm}, 12 \text{ nm}]$), which is validated by experimental process data [6].

Based on the physical mechanisms of ferroelectric polarization and energy storage, the variation of t_{FE} is directly mapped to the key parameters of the LK model (α, β) and C_{FE} through the following formulas.

The Landau coefficient α is closely related to the electric field distribution in the ferroelectric layer. Since the electric field E in the ferroelectric layer satisfies $E \propto 1/t_{FE}$ under a fixed gate voltage, the Landau coefficient α (which reflects the curvature of the Gibbs free energy curve) exhibits an inverse proportional relationship with t_{FE} . The mapping formula is

$$\alpha(t_{FE}) = (\alpha_0 t_{FE,nominal})/t_{FE} \quad (1)$$

where $\alpha_0 = -1.8 \times 10^{11}$ is the calibrated value of α when $t_{FE} = 10$ nm (see Table 1). This formula is derived from the energy balance principle of ferroelectric polarization, ensuring that the negative capacitance effect is maintained within the process window.

The Landau coefficient β describes the quartic term of the Gibbs free energy and is associated with the polarization stiffness of the ferroelectric material. The polarization energy density of the ferroelectric layer is proportional to $1/t_{FE}^2$, leading to a quadratic inverse proportional relationship between β and t_{FE} . The mapping formula is

$$\beta(t_{FE}) = \beta_0 (t_{FE,nominal}/t_{FE}^2) \quad (2)$$

where $\beta_0 = -5.8 \times 10^{22}$ is the calibrated value of β at the nominal t_{FE} (Table 1). This quadratic relationship is verified by the polarization-electric field (P - E) curve fitting results of HZO ferroelectric films [6].

The equivalent small-signal capacitance of the ferroelectric layer is calculated based on the parallel-plate capacitor model, considering the physical dimensions and dielectric properties of the ferroelectric layer:

$$C_{FE}(t_{FE}) = \epsilon_{FE} A / t_{FE} \quad (3)$$

where $\epsilon_{FE} = 25\epsilon_0$ (ϵ_0 is the vacuum permittivity) is the dielectric constant of the HZO ferroelectric material [5], and $A = WL_g$ is the gate area. The channel width $W = 0.0001$ m and gate length $L_g = 3.2 \times 10^{-6}$ m are consistent with the MVS model parameters (Table 2).

The LK-MVS joint compact model proposed in this work is not a mere combination of existing models, but achieves three substantive innovations that distinguish it from conventional LK-based NCFET compact models.

First, we realize charge-conservation-driven deep coupling between the LK ferroelectric dynamic model and the MVS channel conduction model. Unlike existing LK-based models that treat ferroelectric polarization and channel transport as loosely connected modules (e.g., Refs. [11,12]), our framework enforces strict charge continuity at the ferroelectric-insulator interface (Fig. 4(b)). This ensures that the transient polarization dynamics described by the LK equation directly modulates the channel charge density in the

MVS model, and vice versa, eliminating physical inconsistencies between ferroelectric energy storage and carrier transport that plague traditional two-step modeling strategies. This deep coupling provides new insights into how ferroelectric polarization dynamics quantitatively regulates channel carrier injection and transport, rather than treating the two as independent physical processes.

Second, we establish a quantitative variation-propagation mechanism that links t_{FE} fluctuations to circuit-level timing characteristics. Existing LK-based models (e.g., Refs. [6,8]) typically focus on single-device electrical characterization (e.g., I - V curves) without explicitly mapping process variations to model parameters. In contrast, we derive physics-based equations that directly translate t_{FE} variations to Landau coefficients ($\alpha \propto 1/t_{\text{FE}}$, $\beta \propto 1/t_{\text{FE}}^2$) and equivalent small-signal capacitance ($C_{\text{FE}} \propto 1/t_{\text{FE}}$), enabling statistical simulation of DTD variations. Validated by experimental P - E curve fitting ($R^2 = 0.98$, Ref. [5]), this mechanism allows the model to propagate device-level perturbations to circuit-level delay distributions—an essential capability for variation-aware logic design that is lacking in prior works.

Third, we construct a DTCO-compatible closed-loop modeling framework that bridges device parameter optimization and circuit performance evaluation. Conventional LK-based models (e.g., Refs. [9,13]) are primarily used for device characterization, with no feedback path to guide process adjustments. Our model, by quantifying the impact of t_{FE} variations on decoder delay ($C_V = 3\%$ – 7%), enables designers to tune key device parameters (e.g. t_{FE} tolerance, Landau coefficients) based on circuit-level timing requirements. This closed-loop paradigm aligns with contemporary DTCO trends, providing a practical tool for low-voltage NCFET circuit design rather than a purely theoretical model.

These innovations address the core limitations of existing LK-based NCFET compact models, demonstrating that our modeling strategy represents a substantive advancement—rather than incremental combination—by integrating physical rigor, variation awareness, and practical design utility. The model's SPICE compatibility (implemented via Verilog-A) further ensures its applicability to industrial circuit design flows, as validated by the 2-to-4 decoder simulation results (Subsections 3.2 and 3.3).

3 Results and discussion

3.1 DTD variations

The variability of NCFET devices originates from multiple sources, including process-induced fluctuations and intrinsic ferroelectric material characteristics [19–22]. Figs. 5(a) and (b) show that under Monte Carlo simulation, the transfer characteristics (in linear and logarithmic coordinates, respectively) of 100 n-type NCFET samples with t_{FE} fluctuating around 10 nm. Fig. 6(a) presents the threshold-voltage distribution extracted from Fig. 5(b) using the constant-current method, while Fig. 6(b) gives the on-state current distribution directly obtained from Fig. 5(a). Similarly, Figs. 7(a) and (b) display the corresponding transfer characteristics of 100 p-type NCFET samples with t_{FE} fluctuations around 10 nm under Monte Carlo simulation, shown in linear and logarithmic coordinates, respectively. Fig. 8(a) illustrates the threshold-voltage distribution of the p-type devices extracted using the constant-current method from Fig. 7(b), and Fig. 8(b) shows the on-state current distribution directly extracted from Fig. 7(a). All related statistical parameters are extracted and used to quantitatively evaluate the degree of device variability.

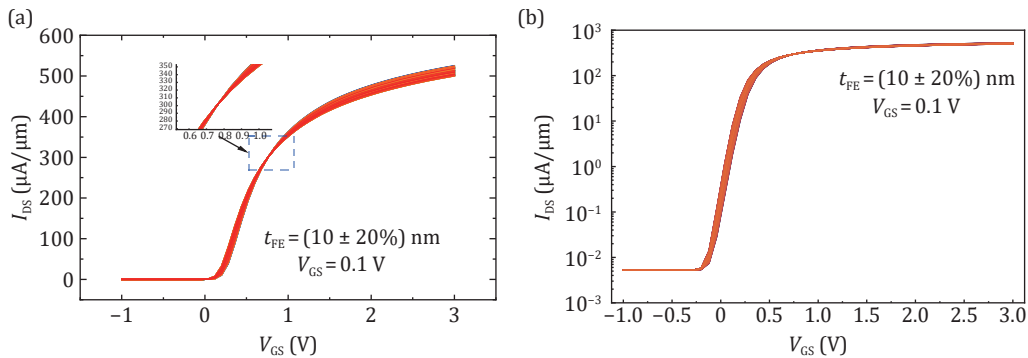


Fig. 5. Transfer characteristics of n-type NCFETs under ferroelectric thickness variation in (a) linear and (b) logarithmic scales.

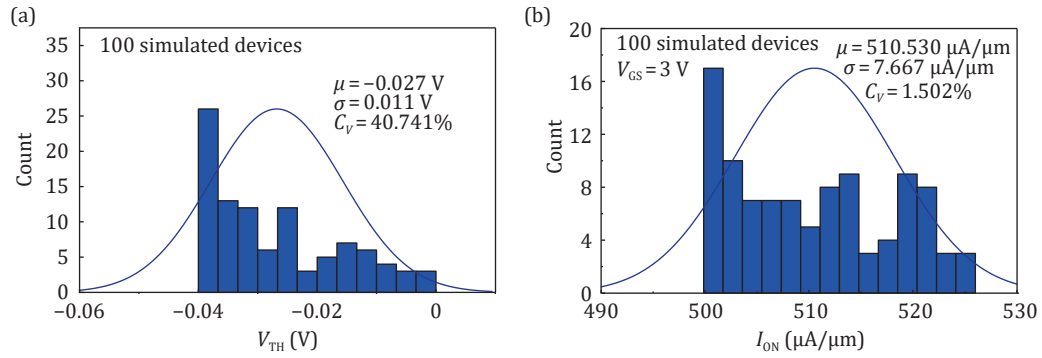


Fig. 6. Statistical distributions of device parameters for 100 simulated n-type NCFETs: (a) histogram of threshold voltage V_{TH} distribution of n-type NCFET and (b) histogram of on-state current distribution I_{ON} of n-type NCFET.

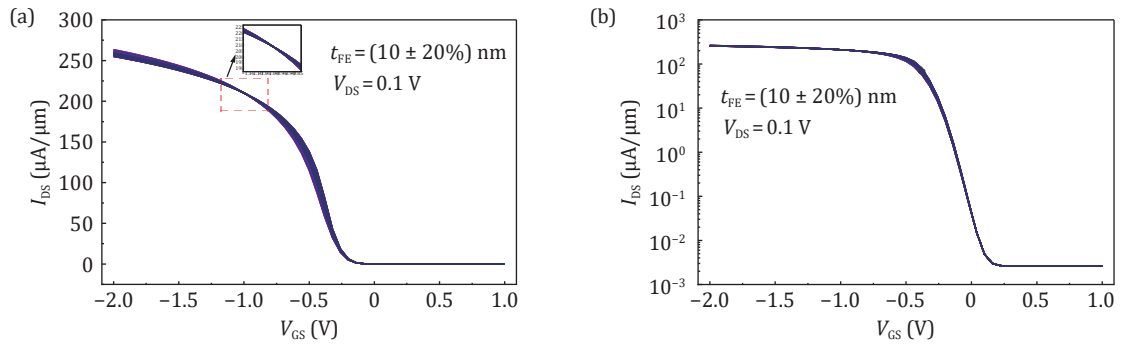


Fig. 7. Transfer characteristics of p-type NCFETs under ferroelectric thickness variation in (a) linear and (b) logarithmic scales.

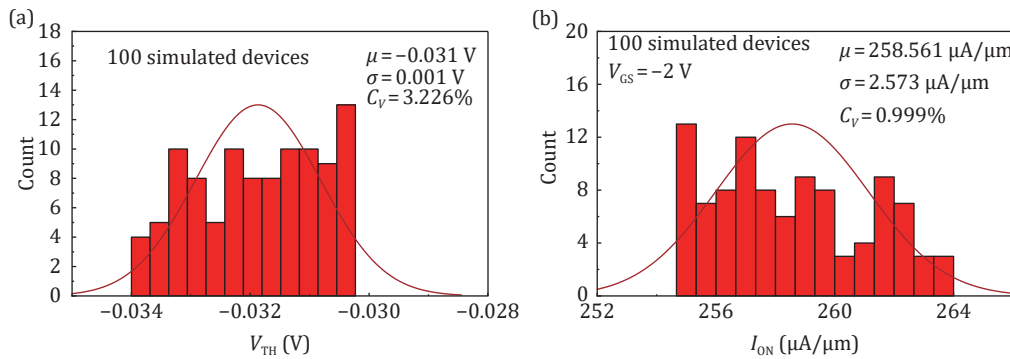


Fig. 8. Statistical distributions of device parameters for 100 simulated p-type NCFETs: (a) histogram of threshold voltage V_{TH} distribution of p-type NCFET and (b) histogram of on-state current I_{ON} distribution of p-type NCFET.

3.2 2-to-4 decoder logic circuits implementation

We further implemented an NC-CMOS 2-to-4 decoder (Fig. 9) in Cadence Virtuoso and performed simulations at $t_{FE} \approx 10$ nm and low V_{DD} (Fig. 10). Each input combination produced a unique enabled output bit, validating the logical correctness of the design. For all four input combinations (00, 01, 10, 11), the circuit generated correct and distinct enable output signals with clear separation between outputs and well-defined dynamic transitions. This not only rigorously verified the complete logical correctness of the decoder but also demonstrated, at the circuit level, the great potential of NC-CMOS technology in maintaining signal integrity and stability for ultra-low-voltage digital logic circuits.

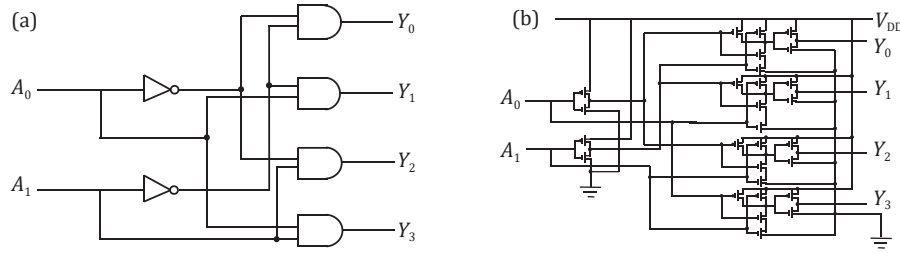


Fig. 9. Schematic diagrams of a 2-to-4 decoder based on NC-CMOS: (a) gate-level and (b) transistor-level.

3.3 Circuit robustness analysis

To evaluate the impact of random t_{FE} fluctuations, which is introduced solely by the ALD process on gate-level timing, we performed 100 Monte Carlo simulations on NCFET inverters/gates near the nominal $t_{FE} \approx 10$ nm, using the method illustrated in Fig. 11 to define and extract high-to-low and low-to-high propagation delays. Figs. 12(a)–(d) show the delay histograms and Gaussian fittings for four representative signal paths, all exhibiting unimodal distributions. The mean values are on the nanosecond scale, with coefficients of variation C_V around 3%–7%, indicating that timing fluctuations are well controlled. Table 3 summarizes the statistical metrics (mean and standard deviation) of the corresponding test points, which can serve as references for subsequent timing budget and margin analysis. Overall, under the scenario considering only t_{FE} thickness variations, NCFET circuits exhibit strong robustness of propagation delay against random manufacturing deviations. However, when t_{FE} deviates from its nominal value or when read/write pulses are shortened, the tail probability of the delay distribution increases, requiring sufficient design margin in layout and gate-level buffering.

To further highlight the robustness advantage of NCFET-based decoders, we compare the delay variation characteristics with reported CMOS and FinFET decoders at the same 14-nm process node [23–25]. For conventional CMOS 2-to-4 decoders operating at sub-1-V V_{DD} , the coefficient of delay variation typically ranges from 8% to 12%, which is attributed to the limited drive strength and significant threshold voltage variation under low-voltage conditions. FinFET decoders reduce the variation to 5%–9% by virtue of improved electrostatic control, but still exhibit higher delay fluctuations than the proposed NCFET decoder ($C_V = 3\% - 7\%$). The superior robustness of the NCFET decoder originates from the intrinsic voltage amplification effect of the ferroelectric layer, which mitigates the impact of t_{FE} variations on effective drive current. Specifically, when t_{FE} decreases by 20%, the negative capacitance effect enhances the gate electric field, compensating for the reduction in ferroelectric layer thickness and suppressing the degradation of transconductance gain. As shown in Table 4,

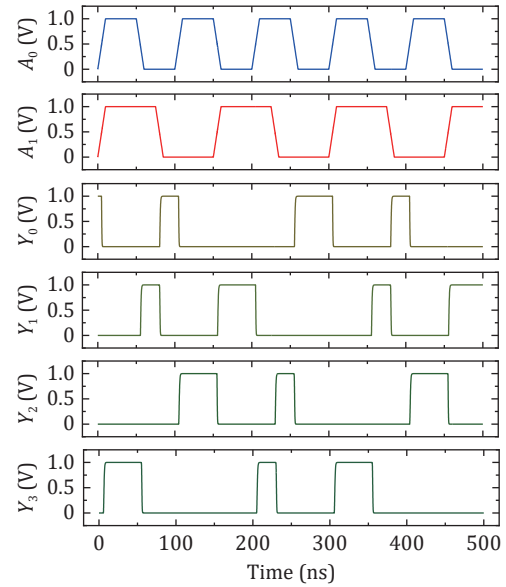


Fig. 10. Logic simulation waveforms of the 2-to-4 decoder with $t_{FE} = 10$ nm.

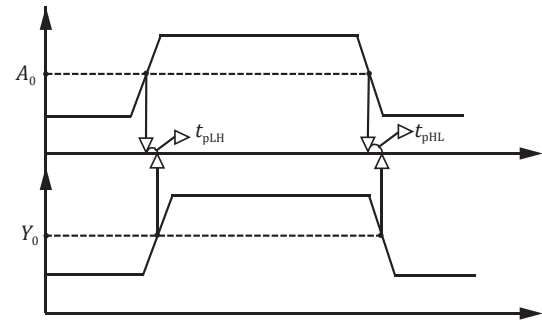


Fig. 11. Schematic diagram of propagation delay measurement.

the propagation-delay values of four output branches are provided for timing-margin assessment. This unique device-level physical mechanism enables NCFETs to achieve better timing stability under process variations, making them more suitable for ultra-low-voltage logic applications.

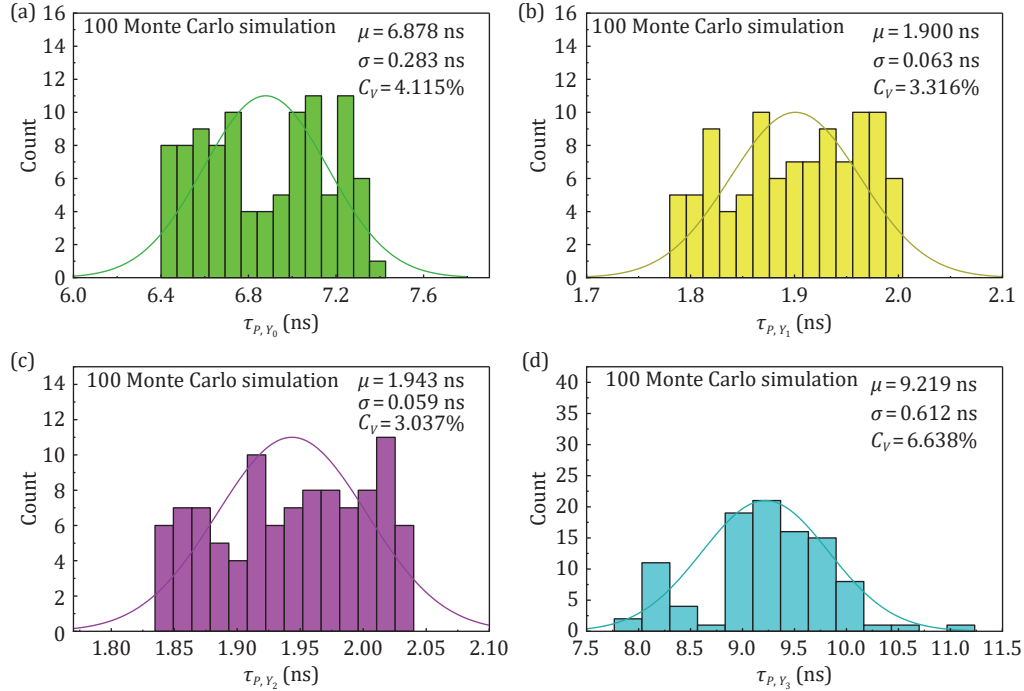


Fig. 12. Histograms of propagation delay τ distributions extracted from simulation: (a) output 0, (b) output 1, (c) output 2, and (d) output 3.

3.4 Discussion

The results presented in Subsections 3.1–3.3 demonstrate the feasibility of the proposed LK–MVS compact model and its utility in evaluating NCFET-based circuits under process variations. Several broader implications emerge from this study, which will be discussed below.

The LK–MVS joint model successfully bridges ferroelectric dynamics and short-channel transport, providing a SPICE-compatible framework that is both physically grounded and computationally efficient. As shown in Fig. 13, the model accurately reproduces experimental I – V characteristics across linear, logarithmic, and output regimes. This confirms its suitability for both device characterization and circuit-level simulation. Moreover, the model's structure, modular, and Verilog-A compatible, enable straightforward extension to more complex architectures, such as metal ferroelectric metal insulator semiconductor (MFMIS) gate stacks or multi-domain ferroelectric systems.

Our Monte Carlo simulations reveal that NCFET-based logic gates exhibit well-behaved delay distributions under t_{FE} fluctuations, with C_V in the range of 3%–7%. This suggests that, for the studied process window ($t_{FE} \approx 10$ nm), NCFETs can maintain timing integrity without excessive design margins. However, it is important to note that other variation sources, such as polarization orientation randomness,

Table 3

Fitted parameters of the MVS model(b).

Parameter	Value
Virtual-source barrier height Φ_b	1.2 V
Body effect coefficient γ	$0.2 V^{\frac{1}{2}}$
Zero-bias threshold voltage V_{t0}	0.5183 V
DIBL coefficient α	3.5
Charge coupling factor CC	0
Drain-dependent swing coefficient n_d	0.39051/V

Table 4

Transmission delay values.

Parameter	Value (s)
t_0	2.04×10^{-7}
t_1	1.58×10^{-7}
t_2	1.50×10^{-7}
t_3	1.28×10^{-7}

grain boundary effects, or interface trap fluctuations, may introduce additional timing tails. Future work should incorporate these factors to form a more complete variation model.

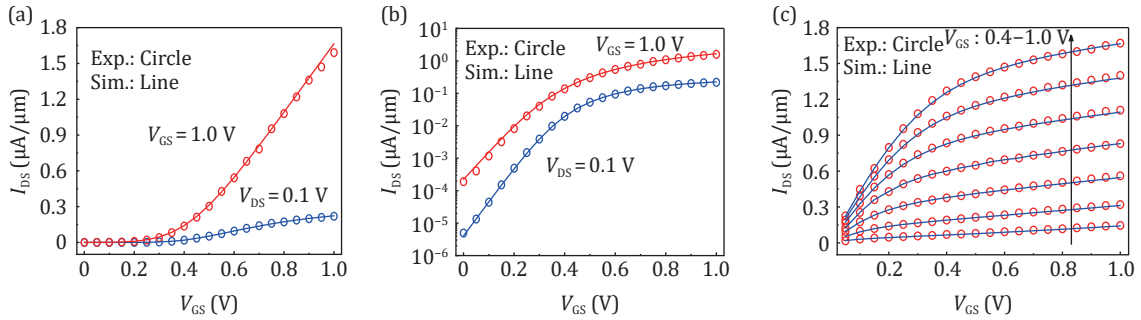


Fig. 13. Fitting results of the MVS model and experimental data: (a) transfer characteristics in linear scale, (b) transfer characteristics in logarithmic scale, and (c) output characteristics.

A key contribution of this work is the “DTD-centric” feedback path from circuit-level timing statistics back to device parameter optimization. By quantifying how t_{FE} variations propagate to decoder delay distributions, designers can make informed trade-offs among performance, power, and robustness. For example, if a tighter delay spread is required, the ferroelectric thickness tolerance can be tightened during fabrication, or Landau coefficients can be tuned via doping or strain engineering. This closed-loop methodology aligns well with the emerging paradigm of DTCO.

While this study focuses on a 2-to-4 decoder as a test vehicle, the proposed framework is readily scalable to more complex digital subsystems, such as SRAM arrays, higher-order decoders, or arithmetic logic units (ALUs). In particular, NCFETs’ intrinsic voltage amplification and steep subthreshold slope make them promising candidates for low-voltage in-memory computing architectures, where peripheral circuits like decoders and sense amplifiers are critical to overall energy efficiency. Future efforts will explore the integration of the proposed NCFET model into standard cell libraries and memory compilers, enabling full-system benchmarking.

Although the current model captures major aspects of NCFET behavior, several extensions are warranted. These include modeling multi-domain switching effects, temperature dependence, and dynamic hysteresis under alternating current (AC) excitation. Additionally, while the MVS model covers short-channel effects well, further calibration against ultra-scaled nodes (e.g., sub-10 nm) will enhance predictive accuracy. From a circuit perspective, the impact of NCFET-specific transient behaviors, such as overshoot and ringing, on dynamic power and signal integrity deserves deeper investigation.

In summary, the LK-MVS joint model and the associated variation-aware simulation framework provide a solid foundation for NCFET-based circuit design. By linking device physics to system-level metrics, this work supports the development of robust, low-voltage digital systems in the post-Moore era.

4 Conclusions

This study has successfully developed and implemented an LK-MVS compact model for NCFETs and integrated it into a SPICE simulation environment. This integration enables a unified framework for evaluating device-level statistical variability, encompassing both intrinsic ferroelectric fluctuations and process-induced variations (DTCO), alongside circuit-level performance metrics such as gate-level delay distribution. This achievement provides a critical bridge from NCFET device physics to practical circuit design.

Using a fundamental 2-to-4 decoder as a test case, we have demonstrated a complete bottom-up, feedback-driven, device-circuit, and co-design methodology. Starting with precise modeling and statistical analysis of NCFET variability, the approach evaluates circuit functional robustness and performance stability under low-voltage and variation-prone conditions. The simulation results are then fed back to the device design stage, offering clear guidance for optimizing key parameters like t_{FE} and Landau coefficients.

The proposed modeling and co-design framework are highly scalable and general, extending beyond simple decoders to support the development of more complex digital systems, such as higher-order decoders

and arithmetic logic units, as well as emerging architectures like NCFET-based in-memory computing macros. This work thus outlines an effective pathway to overcoming circuit-level performance bottlenecks by leveraging intrinsic device-level physical gains.

CRediT authorship contribution statement

Yao-Yu Shi: Writing—original draft, Software, Validation, Investigation, Formal analysis, Data curation, Visualization.
Bin Wang: Writing—review & editing, Conceptualization, Methodology, Supervision, Project administration, Resources.

Declaration of competing interest

The authors declare no conflicts of interest.

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